Cactus® Technologies

An Introduction To SD Card Interface

White Paper CTWP009

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01.0 Introduction

The Secure Digital Card (SD Card, for short) was originally introduced to address the need for reliable data storage in a small form factor for consumer hand-held and portable electronics, such as cellphones, digital cameras, etc. Recently, there has been increasing interest to adopt the SD Card for usage in industrial environments also.

Traditionally, the storage interface for industrial applications has been ATA, either in the form of 2.5" drives or via the TrueIDE mode in PC Card, CF Card or DOM. The SD interface, however, is quite different from ATA. This application note is intended to help those who are new to the SD interface to better understand it's features and usage.

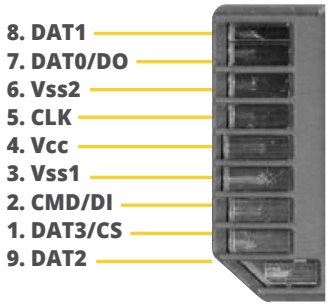
02.0 Specifications

The official SD Specifications is controlled by the SD Card Association **(www.sdcard.org).** This official spec. is available only to SD Card Association members. However, the SD Card Association does make available, for free, a simplified version of the physical layer spec., which is useful to help potential end users to design in the SD Card in their systems. Anyone who is looking to use the SD Card in their design should download this document, as it contains valuable information on the physical interface and command protocols.

03.0 The Basics

Just like the CF Card or PC Card, the SD Card contains an internal controller that handles all internal flash memory operations. The data transfer between the host and the card is done in clock serial mode, in 512 byte blocks. Currently, the defined file system is FAT12/16 for cards that are 2GByte or less in capacity, and FAT32 for cards that are 4GByte or more.

03.1 Pinout



Unlike the CF or PC Card, SD Cards do not use pins for contacts. Instead, the card has 9 contact pads as shown in the picture to the left.

Note the particularity with pad 9 placement and different width for pad 8. This is due to legacy compatibility requirements with MMC Cards.

03.2 Voltage Levels

Standard SD Cards operate at power supply range of 2.7-3.3V. Special low voltage version SD Cards can operate at a power supply level as low as 1.6V. Cactus Technologies SD Cards operate at the standard voltage range.

03.3 Bus Protocols

There are two bus protocols defined for SD Cards. The default mode is native SD mode but the card can be configured to use a slower SPI mode. Protocol selection is done during the first reset command after power up. The SD Card powers up in SD mode. To switch the card to SPI mode, the CS signal must be asserted while the host issues a reset command to the card. Once a particular protocol is configured, it cannot be changed while power is applied. The only way to switch between protocol modes is to do a power cycle.

Information in the remaining sections are for normal SD mode operation. Differences between SD mode and SPI mode are summarized in Section 5.0.

03.4 Bus Width

SD Cards operates in clock serial mode with bit widths of 1-4 bits. In SPI mode, the card operates in 1-bit mode only.

03.5 Clock Frequencies

SD Cards operate at two speed modes. The default mode clock speed is 0-25MHz. A high speed mode is available at clock speed of 0-50MHz.

03.6 Card Registers

All SD Cards contain a set of information registers which describe and control the various features that the cards support. These are similar to the Card Configuration Registers and CIS Structure for PC and CF Cards (or the Identify Drive structure for IDE drives). The following table is a list of the card information registers and their descriptions:

Name	Width	Description
CID	128	Card Identification Number
RCA	16	Relative Card Address; Used Only in SD Mode
DSR	16	Drive Stage Register; This is optional for controlling the card's output drivers
CSD	128	Card Specific Data; this is similar to CIS or Identify Drive structure
SCR	64	SD Configuration Register
OCR	32	Operation Condition Register

04.0 Protocol Basics

SD Card protocol consists of an exchange of command and/or response tokens between the host and the card. Data transfers occurs in packets. A packet consists of a data block and CRC check bits. Data transfer can occur in single block or multiblock mode, similar to ATA RD/WR SECTOR and RD/WR MULTIPLE commands.

All transmissions on the CMD/DAT pins are done with MSB first. Commands and responses are sent on the CMD pin while data transfer is done on the DAT pins.

04.1 Command Token

The format of a command token is as follows:

0	0	Response Content	1

48-BIT RESPONSE TOKEN FORMAT

0	0	Response Content	1

136-BIT RESPONSE TOKEN FORMAT

04.2 Data Packet

There are two types of data packet format. One for normal byte wide data and the other for wide width data which uses a 512 bit data block. Both types of data packets are protected with CRC16.

For normal 512 byte data transfers, the data is transferred least significant byte first but in the individual byte, the data is transmitted MSB first.

Data transfer can be done in 1-bit mode (using DAT0 only) or 4-bit mode (if enabled, using DAT03). When using 4-bit mode, the byte data is formatted such that bit[7:4] are sent on DAT[3:0] followed by bit[3:0] on DAT[3:0]. There are detailed diagrams of the formatting in the simplified SD Spec. from the SD Card Association website.

05.0 SPI Mode Operation

While most of the SD Card's operation is the same whether in SD mode or SPI mode, there are a few differences that need to be pointed out.

- SPI mode uses only 1-bit wide data bus width.
- SPI transfers are byte oriented; all commands and data transfers consists of a series of bytes.
- Two new response tokens are define for SPI mode.
- If the card encounters an error condition during data read, it will respond with an ERROR token in SPI mode rather than a timeout as in SD mode.
- For block writes in SPI mode, the card returns a data response token after receiving each data block.
- For block writes in SPI mode, the data block is preceded with a Start Block Token.
- CRC protection is optional for SPI mode. However, the RESET command is issued while the card is in SD mode, thus, this command must be issued with a valid CRC field.
- Command class 1, 3 and 9 are not supported in SPI mode. The supported commands for a specific class are also different between SPI and SD modes.

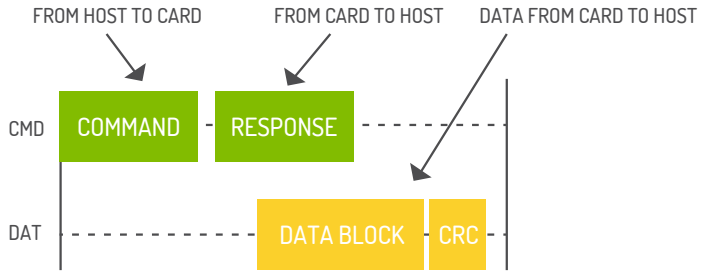
06.0 Further Reading

This white paper is just a simple introduction to the SD Card interface. For more details on the SD protocol, command set, responses, register descriptions, etc., we highly encouraged the reader to download the Simplified SD Card Physical Layer Specifications from the SD Card Association website or obtaining the official full specification by signing the LAMS agreement available from the SD Card Association website.

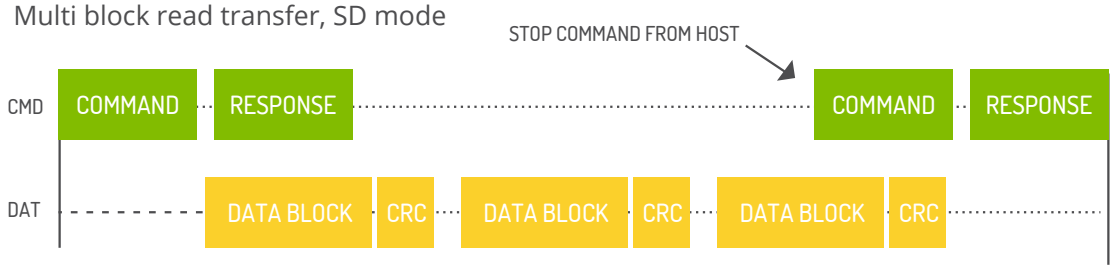
07.0 Appendix

The following are some pictorial representations of data transfer sequences on the SD interface.

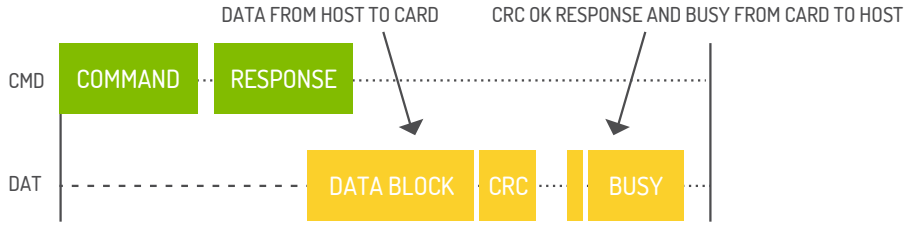
- Single block read transfer, SD mode



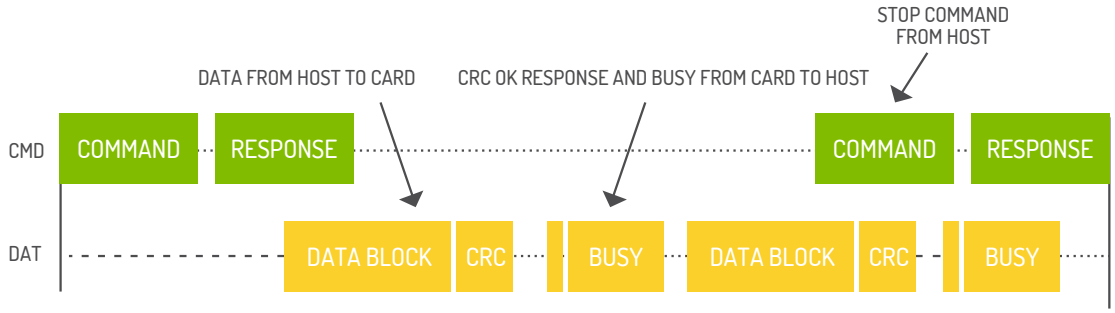
- Multi block read transfer, SD mode



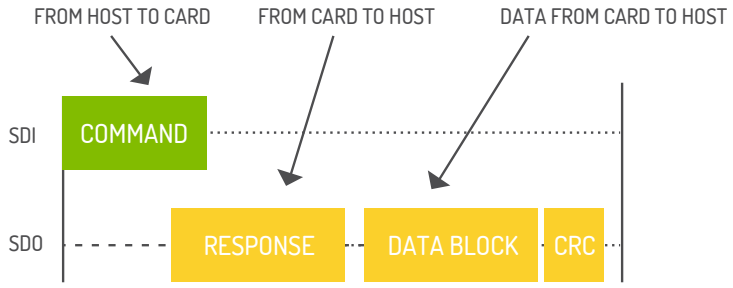
- Single block write transfer, SD mode



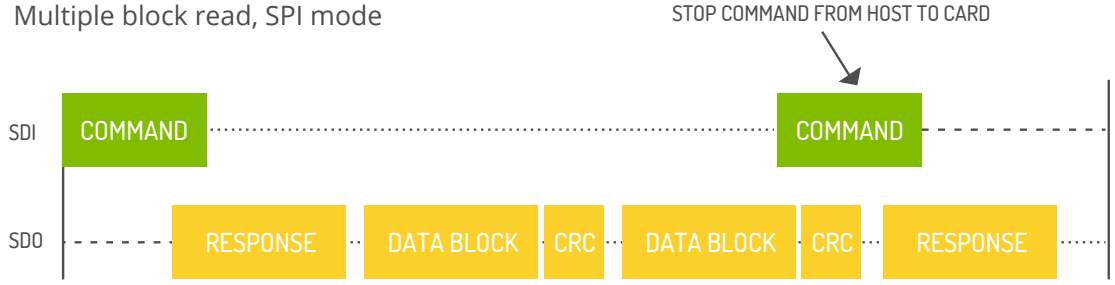
- Multi block write transfer, SD mode



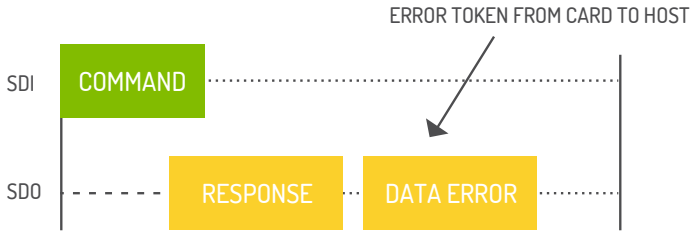
- Single block read, SPI mode



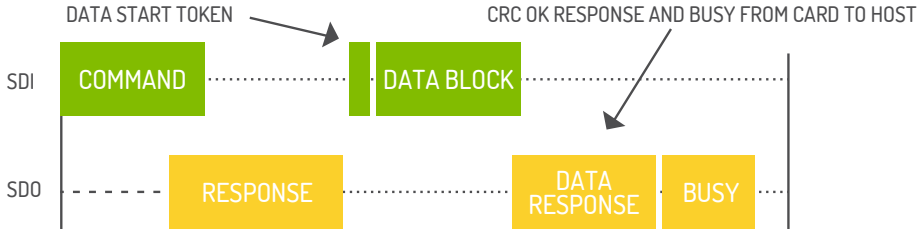
- Multiple block read, SPI mode



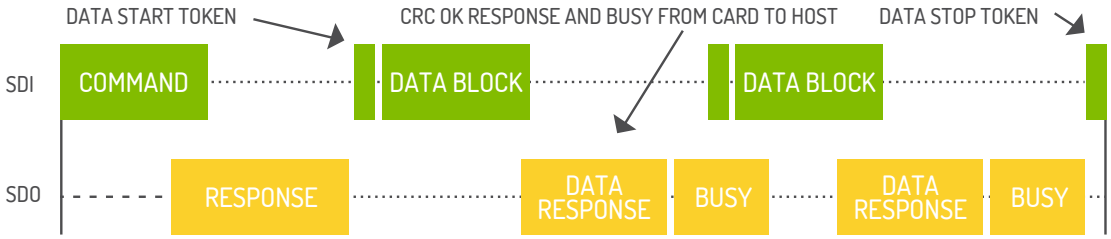
- Block read error response, SPI mode



- Single block write, SPI mode



- Multiple block write, SPI mode



08.0 Support Information

If you would like any additional information regarding data contained in this white paper feel free to contact a Cactus representative:

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