DELKIN DEVICES®

SLC Industrial microSD Memory Card

with

SMART

Engineering Specification

Document Number: L500487

Revision: C

Overview

- **Capacity**
  - SLC 128MB up to 4GB
- **Bus Speed Mode**
  - 128MB~2GB: Non-UHS
  - 4GB: UHS-I
- **Power Consumption**
  - Power Up Current < 250uA
  - Standby Current < 250uA
  - Read Current <200mA
  - Write Current <200mA
- **Performance**
  - Read: Up to 21 MB/s
  - Write: Up to 18 MB/s
- **Advanced Flash Management**
  - Static and Dynamic Wear Leveling
  - Bad Block Management
  - SMART Monitoring
  - Auto-Read Refresh
- **Storage Temperature Range**
  - -40°C ~ 85°C
- **Operation Temperature Range**
  - -40°C ~ 85°C
- **RoHS compliant**

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1. INTRODUCTION

1.1. General Description

Delkin Devices' next generation SLC industrial microSD cards deliver the endurance of SLC, full industrial operating temperature range and total compliance with SD Association Part 1 Physical Layer Specification Version 3.01 standard - in addition to the new SMART functionality, which allows the user to monitor the health of the card directly through host commands or through a simple utility.

Industrial microSD cards are the fastest growing form factor in the storage market, due to their size, robust mechanical design and low power consumption. Delkin has been a leader in this market for years and continues to innovate, providing our customers with new tools to ensure reliable performance.

1.2. Flash Management

1.2.1. Error Correction Code (ECC)

Flash memory cells will deteriorate with use, which might generate random bit errors in the stored data. Thus, the controller in Delkin's SLC industrial microSD cards applies an advanced BCH ECC algorithm, which can detect and correct errors occur during read processes, ensuring data been read correctly, as well as protecting data from corruption.

1.2.2. Wear Leveling

NAND Flash devices can only undergo a limited number of program/erase cycles, and in most cases, the flash media are not used evenly. If some blocks are updated more frequently than others, the lifetime of the device would be reduced significantly. Thus, Wear Leveling techniques are applied to extend the lifespan of NAND Flash by evenly distributing write and erase cycles across the media.

The controller in Delkin's SLC industrial microSD cards utilizes an advanced Wear Leveling algorithm, which can efficiently spread out the flash usage through the whole flash media area. Moreover, by implementing both dynamic and static Wear Leveling algorithms, the life expectancy of the NAND Flash is greatly improved.

1.2.3. Bad Block Management

Bad blocks are blocks that include one or more invalid bits and therefore, their reliability is not guaranteed. Blocks that are identified and marked as bad by the manufacturer are referred to as "Initial Bad Blocks". Blocks that develop invalid bits during the lifespan of the flash are named "Later Bad Blocks". The controller in Delkin's Industrial SLC microSD cards implements an efficient bad block management algorithm to detect the factory-produced bad blocks and manage any bad blocks that appear with use. This practice further prevents data being stored into bad blocks and improves data reliability.

1.2.4. Smart Function

SMART, an acronym for Self-Monitoring, Analysis and Reporting Technology, is a special function that allows a memory device to automatically monitor its health. While there is not an industry standard for SD/microSD card SMART functionality, as there is for SATA & PATA devices, Delkin can provide either an off-line program or commands that can be issued via the host to collect data from the card. Refer to Section 7 for the direct command details and the information that can be extracted from the card.

1.2.5. Auto-Read Refresh

Auto-Read Refresh is a function that is deployed on devices that have heavy read applications and rarely write, such as GPS systems, etc. When blocks are continuously read, the device would not normally trigger wear leveling, since writing and erasing would create the need to wear level. Thus, errors will accumulate and become uncorrectable. Therefore, to avoid the situation where errors will exceed the amount that can be corrected by the controller's ECC engine and then the block will be marked bad, the controller firmware will automatically refresh the bit errors when the error count in a block approaches the ECC threshold.

2. PRODUCT SPECIFICATIONS

- **Capacity**
  - SLC: 128MB~4GB
- **Operation Temp. Range**
  - -40~+85°C
- **Storage Temp. Range**
  - -40~+85°C
- **Support SD system specification version 3.0**
- **Card capacity of non-secure area and secure area support [Part 3 Security Specification Ver3.0 Final] Specifications**
- **Support SD & SPI mode**
- **Designed for read-only and read/write cards**
- **Bus Speed Mode (using 4 parallel data lines)**
  - **Non-UHS mode**
    - Default Speed mode: 3.3V signaling, Frequency up to 25 MHz, up to 12.5 MB/sec
    - High Speed mode: 3.3V signaling, Frequency up to 50 MHz, up to 25 MB/sec

    Note: SDSC card (capacity ≤ 2GB) only supports non-UHS mode.
  - **UHS-I mode**
    - SDR12 - SDR up to 25MHz 1.8V signaling
    - SDR25 - SDR up to 50MHz 1.8V signaling
    - SDR50: 1.8V signaling, Frequency up to 100 MHz, up to 50MB/sec
    - SDR104: 1.8V signaling, Frequency up to 208MHz, up to 104MB/sec
    - DDR50: 1.8V signaling, Frequency up to 50 MHz, sampled on both clock edges, up to 50MB/sec

    Note: Timing in 1.8V signaling is different from that of 3.3V signaling.
- **The command list supports [Part 1 Physical Layer Specification Ver3.1 Final] definitions**
- **Copyright Protection Mechanism**
  - Compliant with the highest security of SDMI standard
- **Supports CPRM (Content Protection for Recordable Media) of SD Card**
- **Card removal during read operation will never harm the content**
- **Password Protection of cards (optional)**

- **Write Protect feature using mechanical switch on SD adapter**
- **Built-in write protection features (permanent and temporary)**
- **+4KV/-4KV ESD protection in contact pads**
- **Operation voltage range: 2.7 ~ 3.6V**

2.1. Part Numbers and Performance

Capacity	Temperature Range	Part Number	Sequential	
			Read (MB/s)	Write (MB/s)
128MB	-40 to +85°C	S312TLKBP-C1000-3	16	4
256MB	-40 to +85°C	S325TLMBP-C1000-3	16	10
512MB	-40 to +85°C	S351TLMBP-C1000-3	21	15
1GB	-40 to +85°C	S30GTLDBP-C1000-3	21	15
2GB	-40 to +85°C	S302TLDBP-C1000-3	21	18
4GB	-40 to +85°C	S304TLDBP-CX000-3	21	18

NOTES:

1. Performance benchmarks measured with TestMetrix.
2. Actual performance in host system may vary depending on computer configuration, application, workload, etc.
3. All capacities below 4GB are non-UHS enabled. 4GB is UHS-I enabled.
4. SD adapters are not included and are sold separately.
   Reference Part # PAK CAS MICROSD ADAPTER BV1

3. ENVIRONMENTAL SPECIFICATIONS

3.1. Environmental Conditions

Temperature and Humidity

- Storage Temperature Range
  - -40°C ~ 85°C
- Operating Temperature Range
  - -40°C ~ 85°C
- Relative Humidity
  - 5 - 95%, non-condensing

Shock & Vibration

- Shock Specification
  - 1500G, 0.5ms duration
- Vibration Specification
  - 80Hz~2000Hz/20G

Electrostatic Discharge (ESD)

- Contact
  - ± 4KV
- Air
  - ± 8KV

EMI Compliance

- FCC: CISPR22
- CE: EN55022
- BSMI 13438

4. SD CARD COMPARISON

Table 4-1 Comparing SD3.0 Standard and SD3.0 SDHC

	SD3.0 Standard (Backward compatible to 2.0 host)	SD3.0 SDHC
Addressing Mode	Byte (1 byte unit)	Block (512 byte unit)
HCS/CCS bits of ACMD41	Supported	Supported
CMD8 (SEND_IF_COND)	Supported	Supported
CMD16 (SET_BLOCKLEN)	Supported	Supported (Only CMD42)
Partial Read	Supported	Not Supported
Lock/Unlock Function	Mandatory	Mandatory
Write Protect Groups	Optional	Not Supported
Supply Voltage 2.0v – 2.7v (for initialization)	Not Supported	Not Supported
Total Bus Capacitance for each signal line	40pF	40pF
CSD Version (CSD_STRUCTURE Value)	1.0 (0x0)	2.0 (0x1)
Speed Class	**Optional**	Mandatory (Class 2 / 4 / 6 / 10)

5. ELECTRICAL SPECIFICATIONS

5.1. Power Consumption

The table below shows the power consumption of Delkin's microSD cards by configuration.

Table 5-1 Power Consumption

Flash Mode	Max. Power Up Current (uA)	Max. Standby Current (uA)	Max. Read Current (mA)	Max. Write Current (mA)
Single Flash[Note1] (1 x 8bit)	150	150	100	100
SDR/DDR	250	250	200	200

NOTE:

1. Data transfer mode is single channel.

5.2. Electrical Specifications

Absolute Maximum Rating

Item	Symbol	Parameter	MIN	MAX	Unit
1	V_{DD}-V_{SS}	DC Power Supply	-0.3	+3.3	V
2	V_{IN}	Input Voltage	V_{SS}-0.3	V_{DD}+0.3	V
4	Ta	Operating Temperature (Diamond)	-40	+85	℃
5	Tst	Storage Temperature	-40	+85	℃
6	V_{DD}	V_{DD} Voltage	2.7	3.6	V

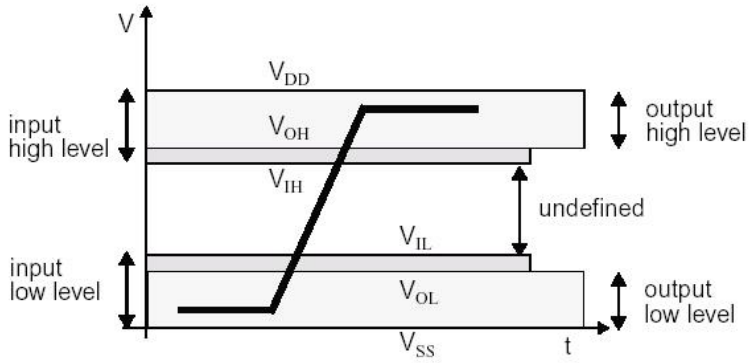
5.3. DC Characteristic

5.3.1. Bus Operation Conditions for 3.3V Signaling

Table 5-2 Threshold Level for High Voltage Range

Parameter	Symbol	Min	Max	Unit	Remarks
Supply voltage	V_{DD}	2.7	3.6	V	
Output High Voltage	VOH	0.75*VDD		V	IOH=-100uA V_{DD}Min.
Output Low Voltage	VOL		0.125*VDD	V	IOL = 100uA VDD min
Input High Voltage	VIH	0.625*VDD	VDD+0.3	V	
Input Low Voltage	VIL	VSS-0.3	0.25 *VDD	V	
Power up time			250	ms	from 0v to VDD min.

Bus Signal Levels



Bus signal levels

Table 5-3 Peak Voltage and Leakage Current

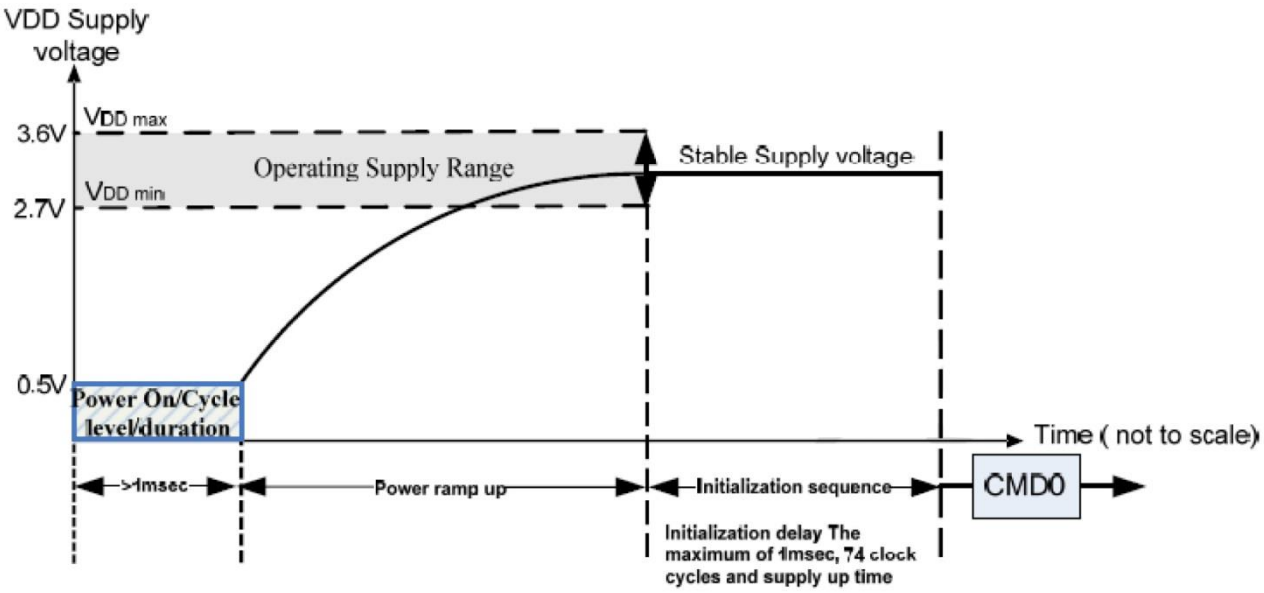
Parameter	Symbol	Min	Max.	Unit	Remarks
Peak voltage on all lines		-0.3	V_{DD}+0.3	V	
All Inputs					
Input Leakage Current		-10	10	uA	
All Outputs					
Output Leakage Current		-10	10	uA	

5.3.2. Bus Signal Line Levels

Parameter	Symbol	Min	Max	Unit	Remark
Pull-up resistance	R_{CMD} R_{DAT}	10	100	kΩ	to prevent bus floating
Total bus capacitance for each signal line	C_L		40	pF	1 card CHOST+CBUS shall not exceed 30 pF
Capacitance of the card for each signal pin	CCARD		10	pF	
Maximum signal line inductance			16	nH	f_{pp}<20 MHz
Pull-up resistance inside card (pin1)	RDAT3	10	90	kΩ	May be used for card detection

5.3.3. Power Up Time

Host needs to keep power line level less than 0.5V and more than 1ms before power ramp up.



Power On or Power Cycle

Followings are requirements for Power on and Power cycle to assure a reliable SD Card hard reset.

(1) Voltage level shall be below 0.5V

(2) Duration shall be at least 1ms.

Power Supply Ramp Up

The power ramp up time is defined from 0.5V threshold level up to the operating supply voltage which is stable between VDD (min.) and VDD (max.) and host can supply SDCLK.

The followings are recommendations for Power ramp up:

(1) Voltage of power ramp up should be monotonic as much as possible.

(2) The minimum ramp up time should be 0.1ms.

(3) The maximum ramp up time should be 35ms for 2.7-3.6V power supply.

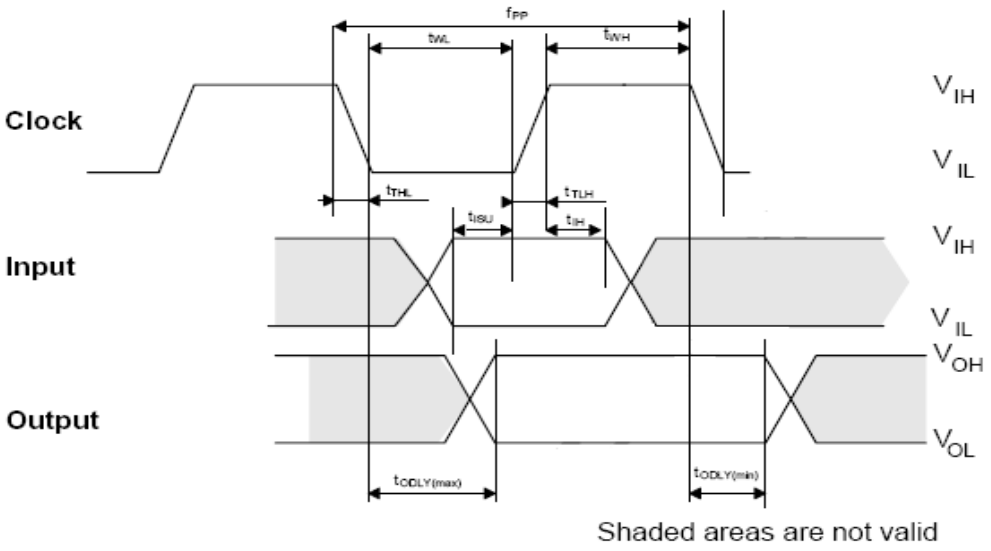
Power Down and Power Cycle

• When the host shuts down the power, the card VDD shall be reduced to less than 0.5Volt for a minimum period of 1ms. During power down, DAT, CMD, and CLK should be disconnected or driven to logical 0 by the host to avoid a situation that the operating current is drawn through the signal lines.

• If the host needs to change the operating voltage, a power cycle is required. Power cycle means the power is turned off and supplied again. Power cycle is also needed for accessing cards that are already in *Inactive State.* To create a power cycle, the host shall follow the power down description before power up the card (i.e. the card VDD shall be once reduced to less than 0.5Volt for a minimum period of 1ms).

5.4. AC Characteristic

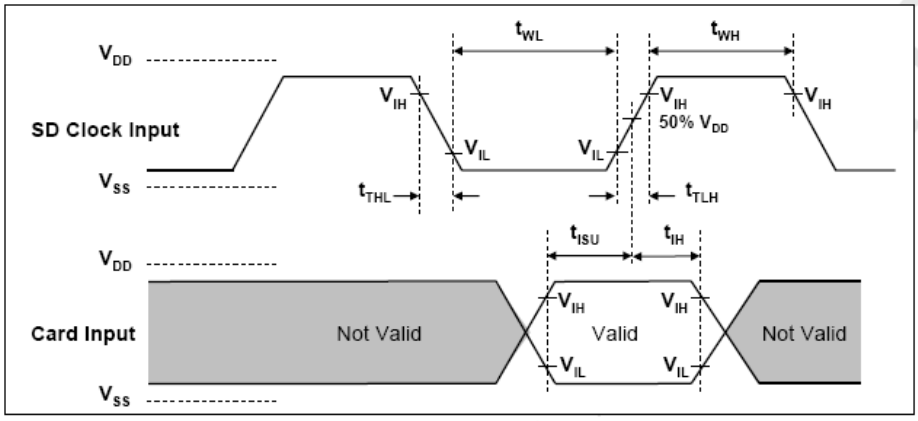
5.4.1. microSD Interface timing (Default)



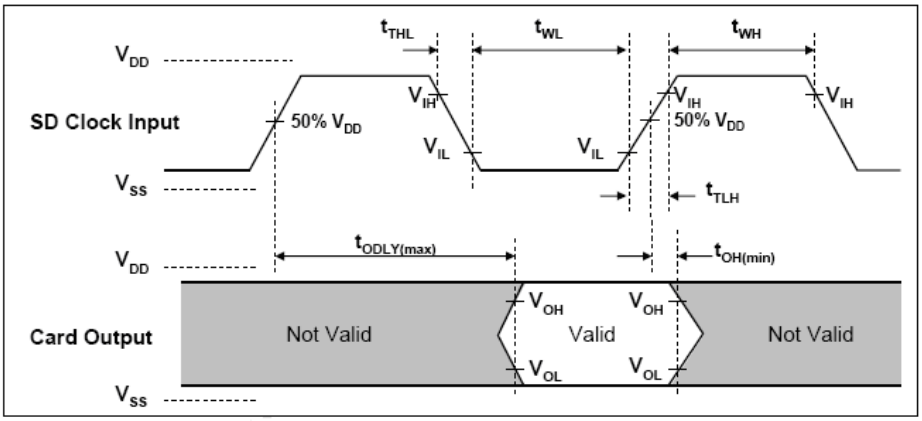
Parameter	Symbol	Min	Max	Unit	Remark
Clock CLK (All values are referred to min(V_{IH}) and max(V_{IL})					
Clock frequency Data Transfer Mode	f_{PP}	0	25	MHz	C_{card}≤□10 pF (1 card)
Clock frequency Identification Mode	f_{OD}	$0_{(1)}$/100	400	kHz	C_{card}≤□10 pF (1 card)
Clock low time	t_{WL}	10		ns	C_{card}≤□10 pF (1 card)
Clock high time	t_{WH}	10		ns	C_{card}≤□10 pF (1 card)
Clock rise time	t_{TLH}		10	ns	C_{card}≤□10 pF (1 card)
Clock fall time	t_{THL}		10	ns	C_{card}≤□10 pF (1 card)
Inputs CMD, DAT (referenced to CLK)					
Input set-up time	t_{ISU}	5		ns	C_{card}≤□10 pF (1 card)
Input hold time	t_{IH}	5		ns	C_{card}≤□10 pF (1 card)
Outputs CMD, DAT (referenced to CLK)					
Output Delay time during Data Transfer Mode	t_{ODLY}	0	14	ns	C_L≤40 pF (1 card)
Output Delay time during Identification Mode	tODLY	0	50	ns	C_L≤40 pF (1 card)

(1) 0Hz means to stop the clock. The given minimum frequency range is for cases were continues clock is required.

5.4.2. microSD Interface Timing (High-Speed Mode)



Card Input Timing (High Speed Card)



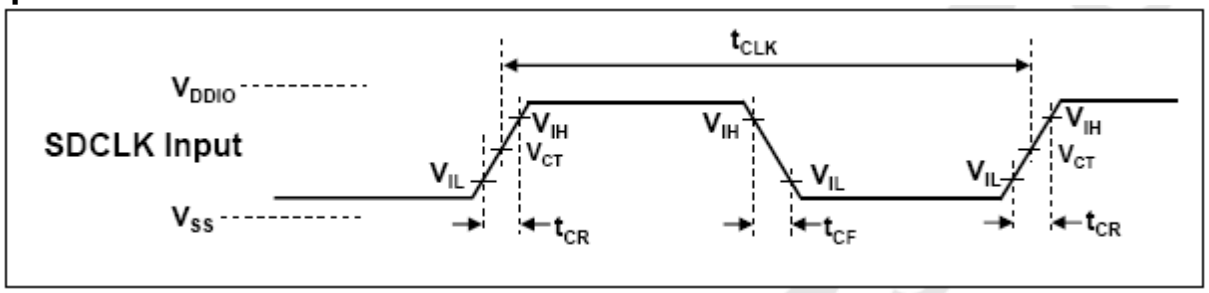
Card Output Timing (High Speed Mode)

Parameter	Symbol	Min	Max	Unit	Remark
Clock CLK (All values are referred to min(V_{IH}) and max(V_{IL})					
Clock frequency Data Transfer Mode	f_{PP}	0	50	MHz	C_{card} ≤ 10 pF (1 card)
Clock low time	t_{WL}	7		ns	C_{card} ≤ 10 pF (1 card)
Clock high time	t_{WH}	7		ns	C_{card} ≤ 10 pF (1 card)
Clock rise time	t_{TLH}		3	ns	C_{card} ≤ 10 pF (1 card)
Clock fall time	t_{THL}		3	ns	C_{card} ≤ 10 pF (1 card)
Inputs CMD, DAT (referenced to CLK)					
Input set-up time	t_{ISU}	6		ns	C_{card} ≤ 10 pF (1 card)
Input hold time	t_{IH}	2		ns	C_{card} ≤ 10 pF (1 card)
Outputs CMD, DAT (referenced to CLK)					
Output Delay time during Data Transfer Mode	t_{ODLY}		14	ns	C_L ≤ 40 pF (1 card)
Output Hold time	T_{OH}	2.5		ns	C_L ≤ 15 pF (1 card)
Total System capacitance of each line[1]	C_L		40	pF	CL ≤ 15 pF (1 card)

(1) In order to satisfy severe timing, the host shall drive only one card.

5.4.3. microSD Interface timing (SDR12, SDR25, SDR50 and SDR104 Modes)

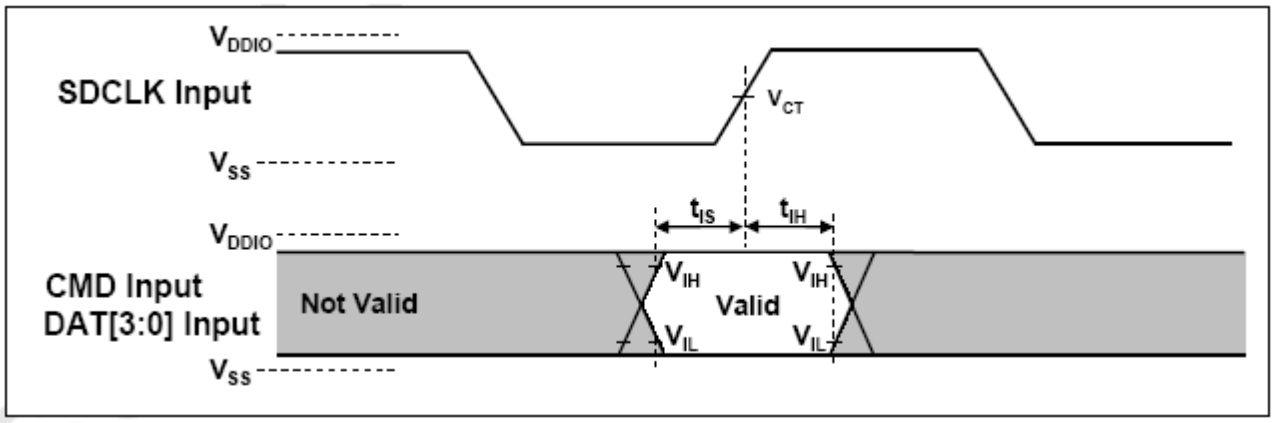
Input:



Symbol	Min	Max	Unit	Remark
tCLK	4.80	-	ns	208MHz (Max.), Between rising edge, VCT= 0.975V
tCR, tCF	-	0.2* tCLK	ns	tCR, tCF < 2.00ns (max.) at 100MHz, CCARD=10pF
Clock Duty	30	70	%	

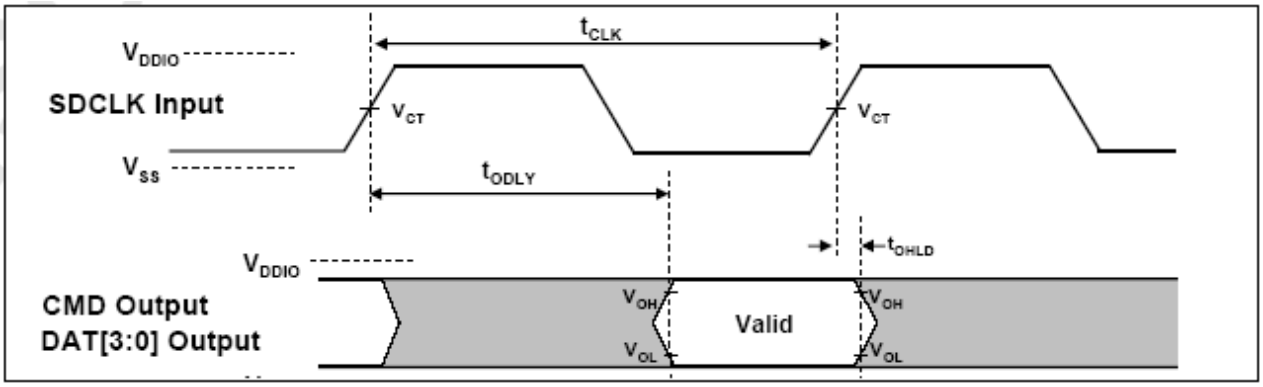
Clock Signal Timing

SDR50 and SDR104 Input Timing:



Symbol	Min	Max	Unit	SDR104 Mode
tIs	1.40	-	ns	CCARD =10pF, VCT= 0.975V
tIH	0.80	-	ns	CCARD =5pF, VCT= 0.975V
Symbol	**Min**	**Max**	**Unit**	**SDR50 Mode**
tIs	3.00	-	ns	CCARD =10pF, VCT= 0.975V
tIH	0.80	-	ns	CCARD =5pF, VCT= 0.975V

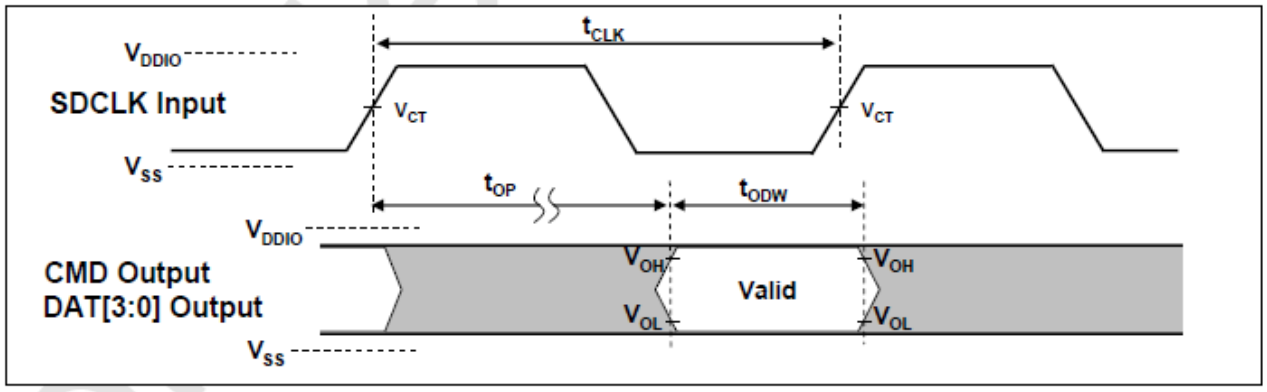
Output Timing of Fixed Data Window (SDR12, SDR25 and SDR50):



Symbol	Min	Max	Unit	Remark
tODLY	-	7.5	ns	tCLK>=10.0ns, CL=30pF, using driver Type B, for SDR50
tODLY	-	14	ns	tCLK>=20.0ns, CL=40pF, using driver Type B, for SDR25 and SDR12,
TOH	1.5	-	ns	Hold time at the tODLY (min.), CL=15pF

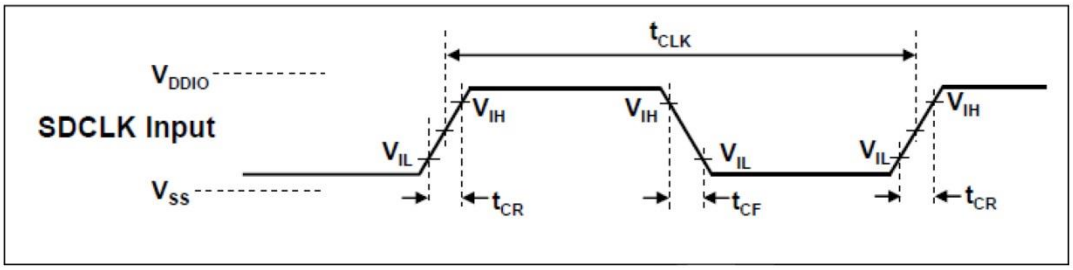
Output Timing of Fixed Data Window

Output Timing of Variable Window (SDR104):



Symbol	Min	Max	Unit	Remark
tOP	0	2	UI	Card Output Phase
ΔtOP	-350	+1550	ps	Delay variable due to temperature change after tuning
tODW	0.60	-	UI	tODW=2.88ns at 208MHz

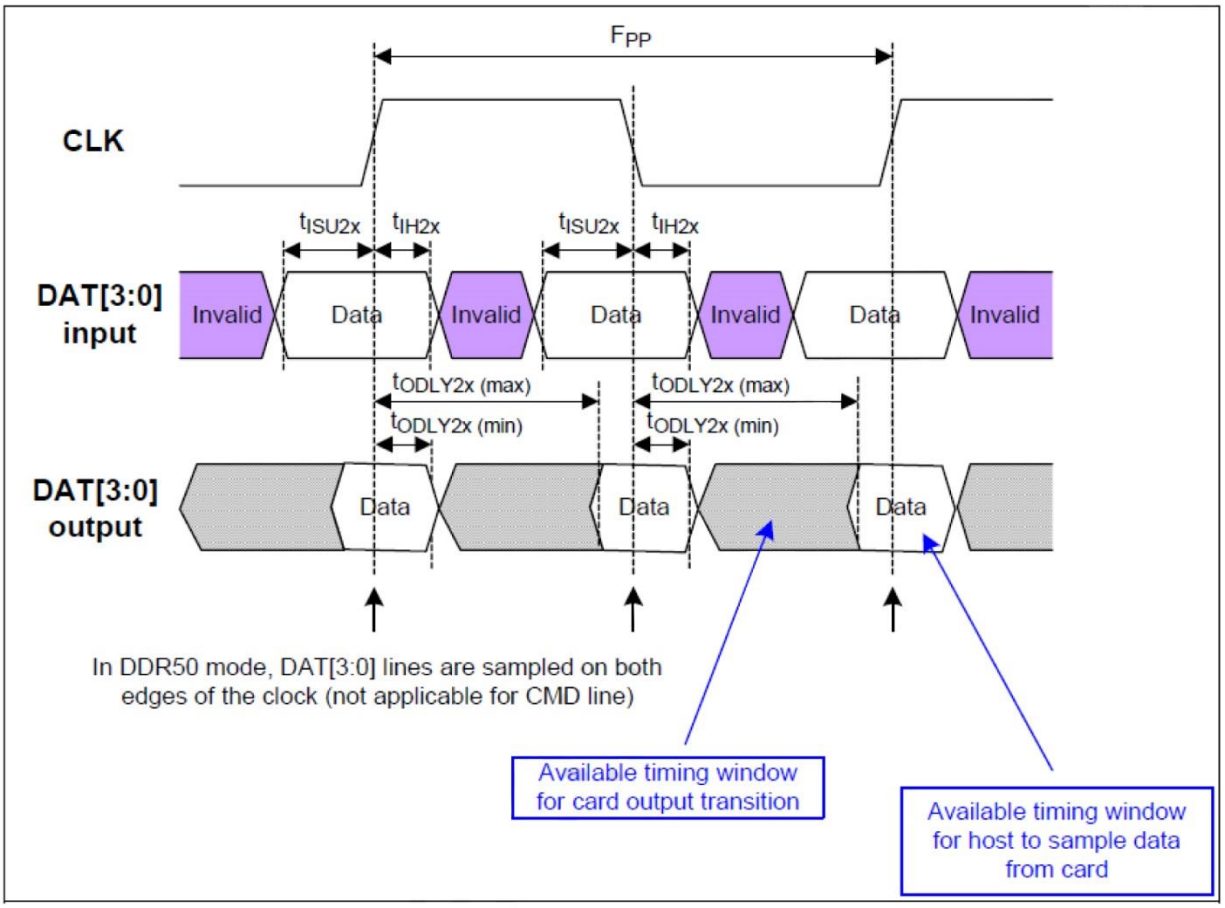
5.4.4. microSD Interface timing (DDR50 Modes)



Clock Signal Timing

Symbol	Min	Max	Unit	Remark
tCLK	20	-	ns	50MHz (Max.), Between rising edge
tCR, tCF	-	0.2* tCLK	ns	tCR, tCF < 4.00ns (max.) at 50MHz, CCARD=10pF
Clock Duty	45	55	%	

Clock Signal Timing



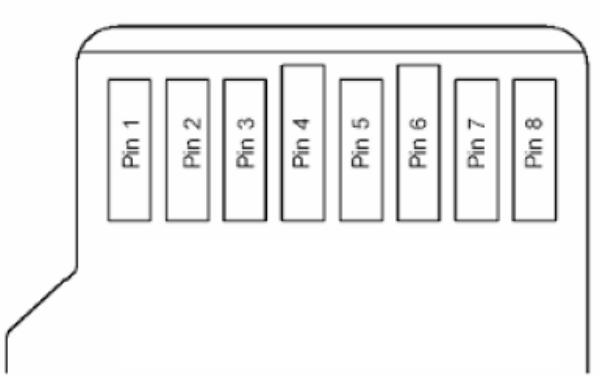
Timing Diagram DAT Inputs/Outputs Referenced to CLK in DDR50 Mode

Parameter	Symbol	Min	Max	Unit	Remark
Input CMD (referenced to CLK rising edge)					
Input set-up time	t_{ISU}	6	-	ns	C_{card}≤ 10 pF (1 card)
Input hold time	t_{IH}	0.8	-	ns	C_{card}≤ 10 pF (1 card)
Output CMD (referenced to CLK rising edge)					
Output Delay time during Data Transfer Mode	t_{ODLY}		13.7	ns	C_L≤30 pF (1 card)
Output Hold time	T_{OH}	1.5	-	ns	C_L≥15 pF (1 card)
Inputs DAT (referenced to CLK rising and falling edges)					
Input set-up time	t_{ISU2x}	3	-	ns	C_{card}≤ 10 pF (1 card)
Input hold time	t_{IH2x}	0.8	-	ns	C_{card}≤ 10 pF (1 card)
Outputs DAT (referenced to CLK rising and falling edges)					
Output Delay time during Data Transfer Mode	t_{ODLY2x}	-	7.0	ns	C_L≤25 pF (1 card)
Output Hold time	T_{OH2x}	1.5	-	ns	C_L≥15 pF (1 card)

Bus Timings – Parameters Values (DDR50 mode)

6. INTERFACE

6.1. Pad Assignment and Descriptions



pin	SD Mode			SPI Mode		
	Name	Type[1]	Description	Name	Type	Description
1	DAT2	I/O/PP	Data Line[bit2]	RSV		
2	CD/DAT3[2]	I/O/PP[3]	Card Detect/ Data Line[bit3]	CS	I[3]	Chip Select (neg true)
3	CMD	PP	Command/Response	DI	I	Data In
4	V_{DD}	S	Supply voltage	V_{DD}	S	Supply voltage
5	CLK	I	Clock	SCLK	I	Clock
6	V_{SS}	S	Supply voltage ground	V_{SS}	S	Supply voltage ground
7	DAT0	I/O/PP	Data Line[bit0]	DO	O/PP	Data Out
8	DAT1	I/O/PP	Data Line[bit1]	RSV		

(1) S: power supply, I: input; O: output using push-pull drivers; PP:I/O using push-pull drivers

(2) The extended DAT lines (DAT1-DAT3) are input on power up. They start to operate as DAT lines after SET_BUS_WIDTH command. The Host shall keep its own DAT1-DAT3 lines in input mode, as well, while they are not used. It is defined so, in order to keep compatibility to MultiMedia Cards.

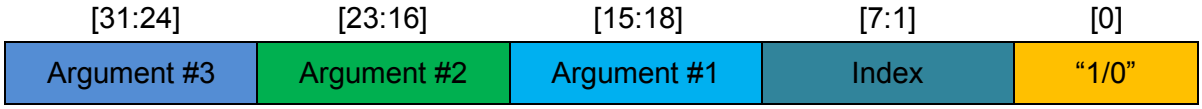
(3) At power up this line has a 50KOhm pull up enabled in the card. This resistor serves two functions - Card detection and Mode Selection. For Mode Selection, the host can drive the line high or let it be pulled high to select SD mode. If the host wants to select SPI mode it should drive the line low. For Card detection, the host detects that the line is pulled high. This pull-up should be disconnected by the user during regular data transfer period, with SET_CLR_CARD_DETECT (ACMD42) command.

Name	Width	Description
CID	128bit	Card identification number; card individual number for identification. **Mandatory**
RCA[1]	16bit	Relative card address; local system address of a card, dynamically suggested by the card and approved by the host during initialization. **Mandatory**
DSR	16bit	Driver Stage Register; to configure the card's output drivers. **Optional**
CSD	128bit	Card Specific Data; information about the card operation conditions. **Mandatory**
SCR	64bit	SD Configuration Register; information about the SD Memory Card's Special Features capabilities **Mandatory**
OCR	32bit	Operation conditions register. **Mandatory.**
SSR	512bit	SD Status; information about the card proprietary features **Mandatory**
OCR	32bit	Card Status; information about the card status **Mandatory**

7. SMART

7.1. Direct Host Access to SMART Data via SD General Command (CMD56)

CMD 56 is structured as a 32-bit argument. The implementation of the general purpose functions will arrange the CMD56 argument into the following format:



Bit [0] Indicates Read Mode when bit is set to [1] or Write Mode when bit is cleared [0]. Depending on the function, either Read Mode or Write Mode can be used.

Bit [7:1] Indicates the index of the function to be executed:

- Read Mode
  - Index = 0x10 Get SMART Command Information
- Write Mode
  - Index = 0x08 Pre-Load SMART Command Information

Bit [15:8] Function argument #1 (1-byte)

Bit [23:16] Function argument #2 (1-byte)

Bit [31:24] Function argument #3 (1-byte)

7.1.1. Process for Retrieving SMART Data

STEP 1:

Write Mode – [0x08] Pre-Load SMART Command Information

Sequence	Command	Argument	Expected Data
Pre-Load SMART Command Information	CMD56	[0] "0" (Write Mode) [1:7] "0001 000" (Index = 0x08) [8:511] All '0' (Reserved)	No Expected Data

STEP 2:

Read Mode – [0x10] Get SMART Command Information

Sequence	Command	Argument	Expected Data
Get SMART Command Information	CMD56	[0] "1" (Read Mode) [1:7] "0010 000" (Index = 0x10) [8:511] All '0' (Reserved)	1 sector (512 bytes) of response data Byte [0-8] Flash ID Byte [9-10] IC Version Byte [11-12] FW Version Byte [13] Reserved Byte [14] CE Number Byte [15] Reserved Byte [16-17] Maximum Bad Block Replacement Byte [18] Reserved Byte [32-63] Bad Block Count per CE Byte [64-65] Good Block Rate (%) Byte [66-79] Reserved Byte [80-83] Total Erase Count Byte [84-95] Reserved Byte [96-97] Calculated Remaining Life (%) Byte [98-99] Average Erase Count Byte [100-101] Minimum Erase Count Byte [102-103] Maximum Erase Count Byte [104-111] Reserved Byte [112-115] Power Cycle Count Byte [116-127] Reserved Byte [128-129] Abnormal Power Down Count Byte [130-159] Reserved Byte [160-161] Total Refresh Count Byte [176-183] Product "Marker" Byte [184-511] Reserved

Note: Both steps are required to retrieve SMART data - Pre-Load SMART Command followed by Get SMART Command, and must be in accordance with the SD Association standard flowchart for CMD56 (below.)

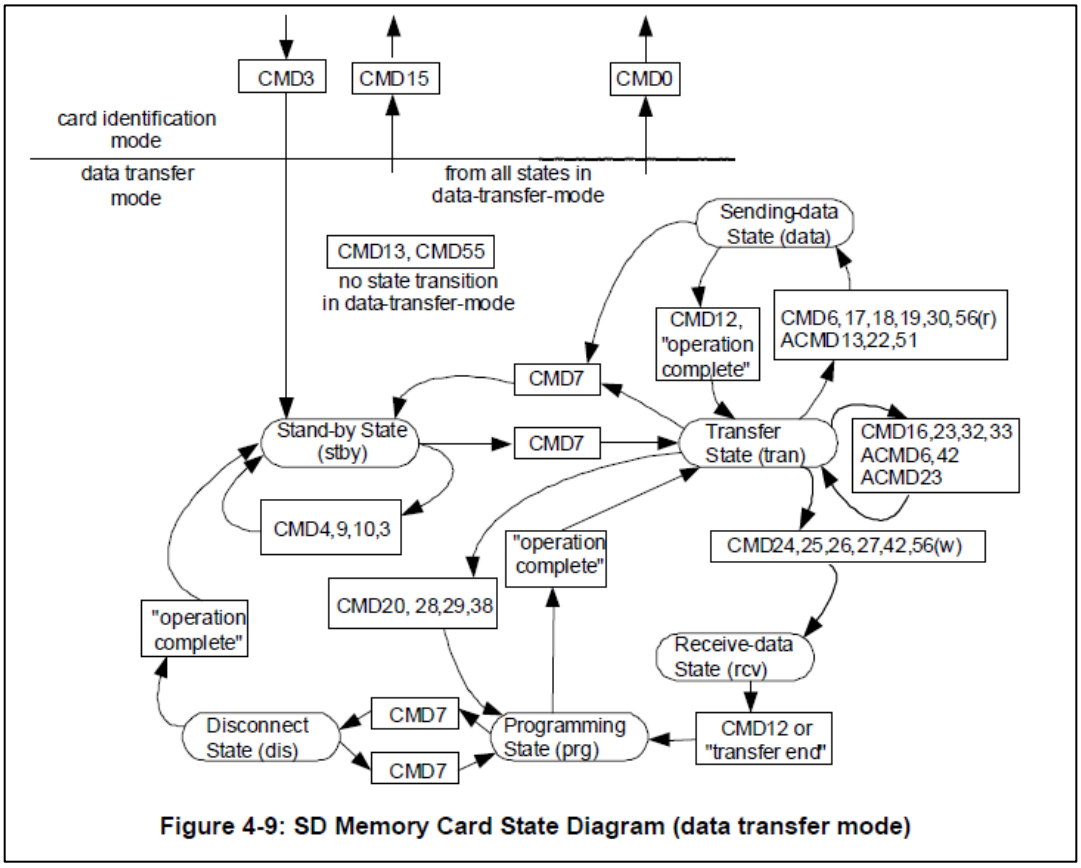


Figure 4-9: SD Memory Card State Diagram (data transfer mode)

Extracted from the SD Specifications Part 1 Physical Layer Simplified Specification Version 3.01.

7.1.2. Definitions for Response Data Bytes

Response Data	Description
Flash ID	NAND Flash Type
IC Version	Controller Version
FW Version	Firmware Version
CE Number	Number of chip enables active
Maximum Bad Block Replacement	Number of spare blocks remaining
Bad Block Count per CE	Number of initial & new bad blocks per chip enable
Good Block Rate (%)	Percent of total blocks that are still marked good
Total Erase Count	Total number of block erases at the card level
Calculated Remaining Card Life	[(Rated P/E cycles – Current Erase Count) / Rated P/E Cycles] * 100%
Average Erase Count	Average erase count over all blocks
Minimum Erase Count	Minimum erase count over all blocks
Maximum Erase Count	Maximum erase count over all blocks
Power Cycle Count	Number of normal power up sequences
Abnormal Power Down Count	Number of unexpected power interruptions
Total Refresh Count	Total read refresh count
Product “Marker”	Product type

7.2. Direct Host Access via DLL for Windows or Linux Operating Systems

Note: Card must be in Idle state before and while accessing card as per steps below.

API entry:

```
int Get_Smart_Data(char drive_letter, unsigned char *buffer, int buffer_len, int *bytes_read);
```

Arguments:

1: Drive letter is a character of the drive letter, i.e. ‘E’
2: buffer is a pointer to a pre-allocated array to store SMART data, min 512 bytes
3: buffer_len indicates to the API the size of the buffer, typically it is 512 bytes
4: bytes_read indicates the number of bytes returned in the buffer

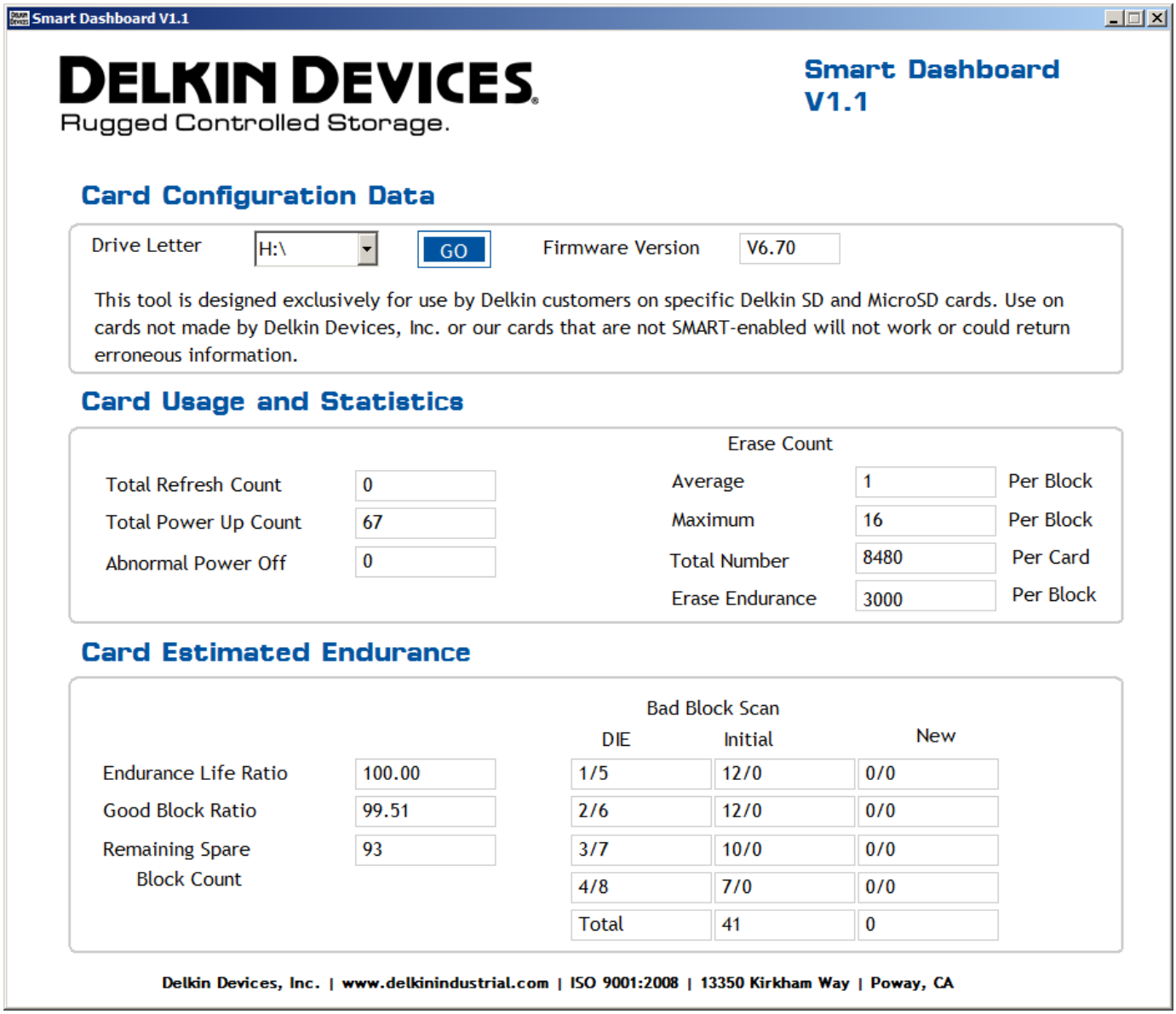
Return Value:

0 is success; Non zero is fail, with the following definitions:

1: "Initial Command Flow Fail"
2: "Read Capacity Fail"
3: "Switch To Vendor Mode Fail"
4: "Send Smart Info Command Fail"
5: "Get Command Response Fail"
6: "Command Response Info Incorrect"
7: "Read Command Info Fail"
8: "Check Command State Fail"
9: "Close Command Flow Fail"

7.3. Access via Delkin SMART Dashboard Utility

Delkin customers will be able to download the Delkin SMART dashboard utility (for Windows OS only) at www.delkinindustrial.com on the Engineering Specification page, or by contacting your Delkin Devices Account Manager. SMART data is accessed by inserting a card in a USB reader or directly in a laptop SD slot (with an SD adapter.) Below is a screen shot of the dashboard with sample data:



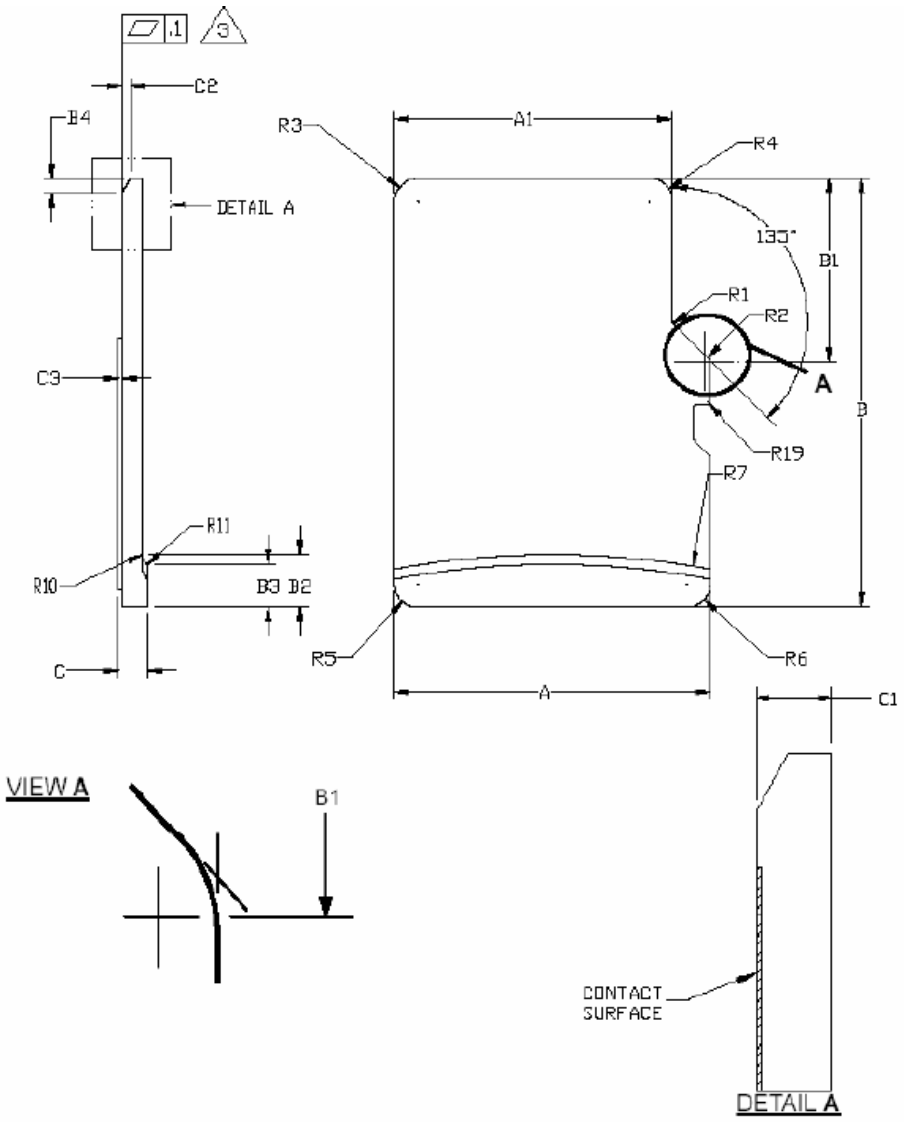
Instructions for use:

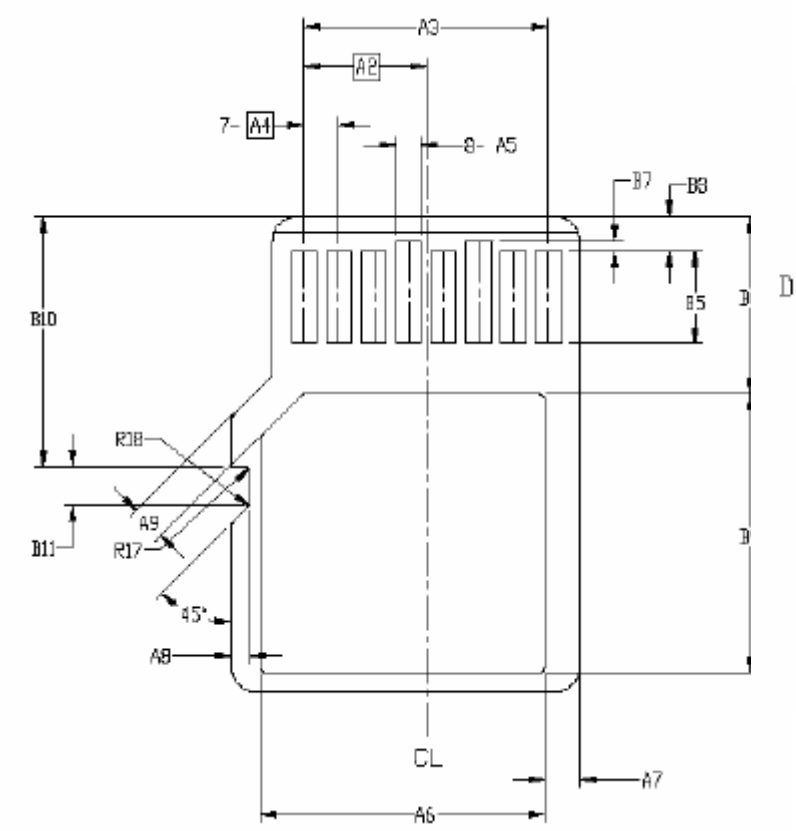
1. Insert microSD in card reader or in SD slot on laptop (in SD adapter)
2. Select appropriate drive letter on Dashboard
3. Click “Go”

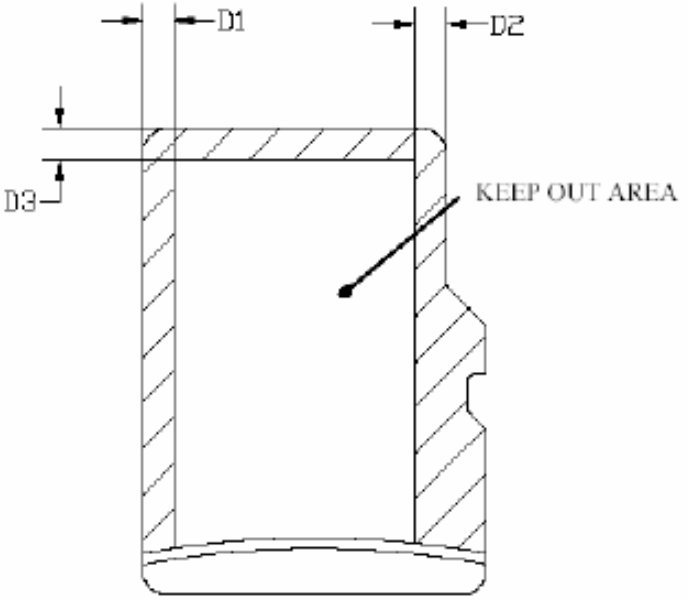
7.3.1. Dashboard Field Descriptions

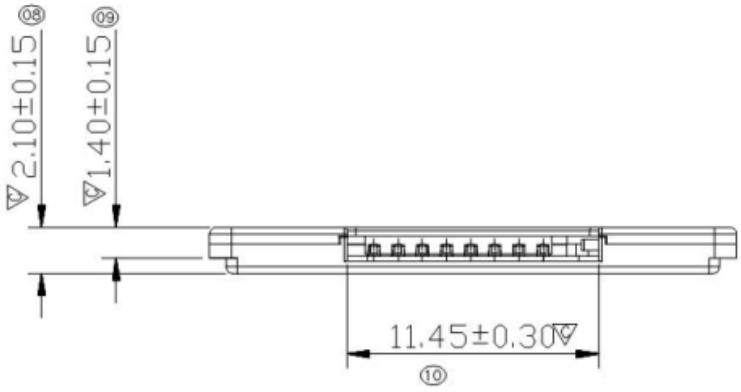
Response Data	Description
FW Version	Firmware Version
Total Refresh Count	Total read refresh count
Total Power Up Count	Number of normal power up sequences
Abnormal Power Off	Number of unexpected power interruptions
Average Erase Count	Average erase count over all blocks
Maximum Erase Count	Maximum erase count over all blocks
Total Erase Count	Total number of block erases at the card level
Erase Endurance	Flash program / erase cycle rating per block
Endurance Life Ratio	[(Rated P/E cycles – Current Erase Count) / Rated P/E Cycles] * 100%
Good Block Ratio	Percent of total blocks that are still marked good
Remaining Spare Block Count	Number of spare blocks remaining
Bad Block Scan - Initial (per die)	Bad blocks in flash from inception, prior to card use
Bad Block Scan - New (per die)	Bad blocks created after card use

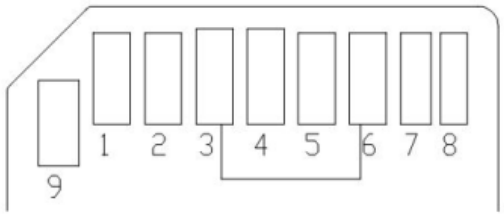
8. PHYSICAL DIMENSIONS



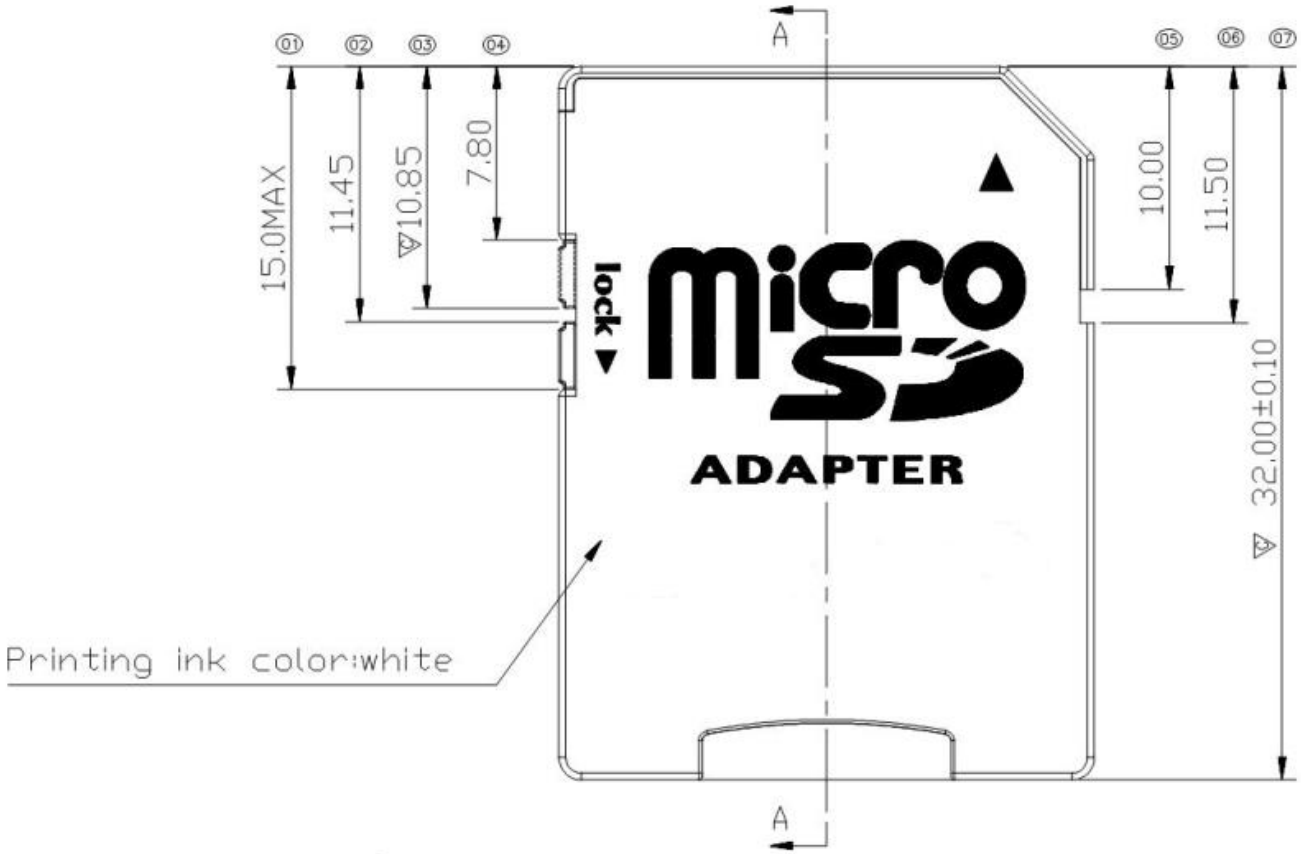


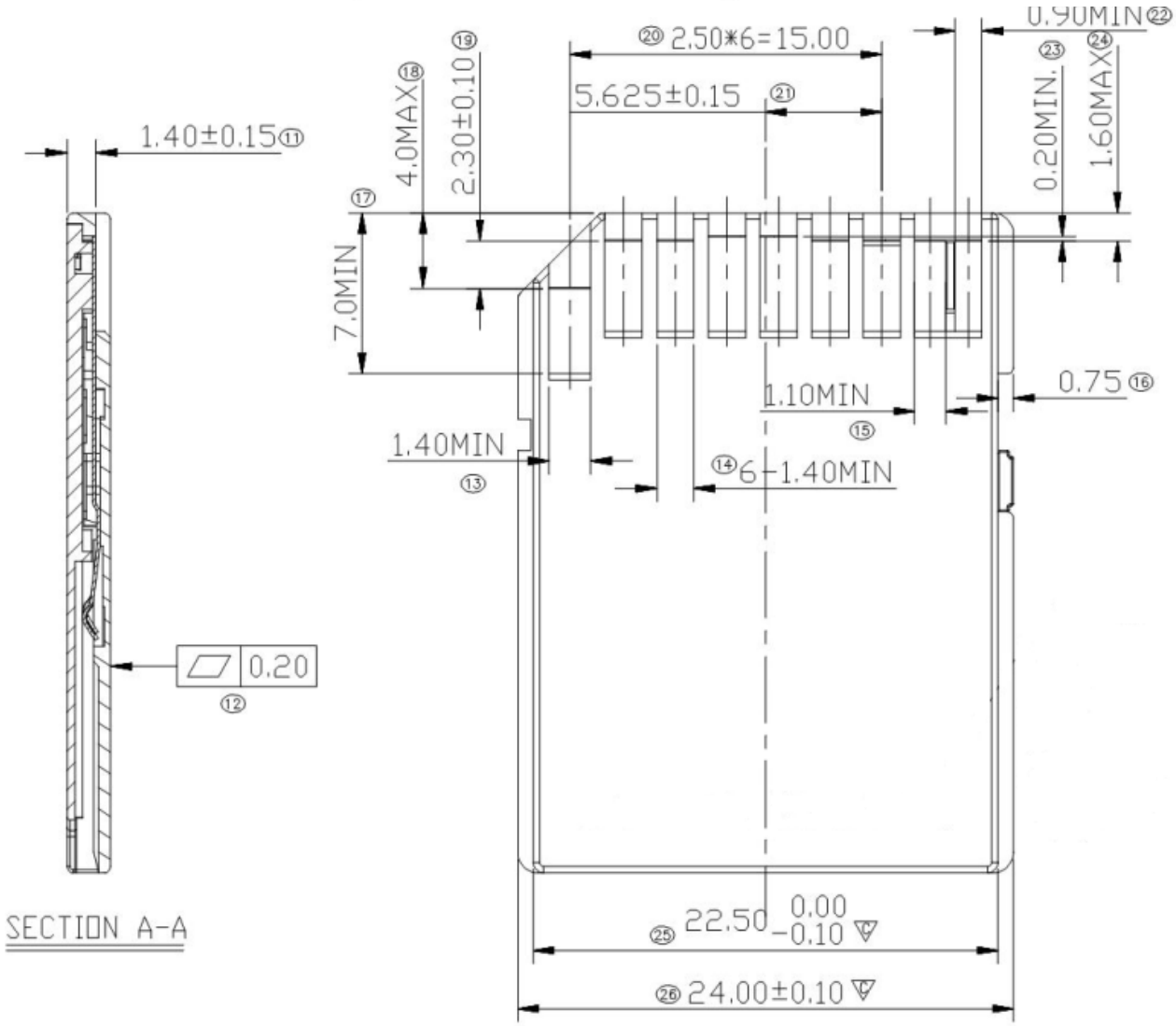






PIN 3 MUST BE CONNECTED TO PIN 6


01
02
03
04
05
06
07
A
15.0MAX
11.45
▽10.85
7.80
10.00
11.50
▽ 32.00±0.10
lock
ADAPTER
Printing ink color:white
A


1.40±0.15⑪
0.20
⑫
SECTION A-A
⑳2.50*6=15.00
5.625±0.15 ㉑
0.90MIN㉒
㉓0.20MIN.
㉔1.60MAX
⑲2.30±0.10
⑱4.0MAX
⑰
7.0MIN
1.10MIN
⑮
0.75⑯
1.40MIN
⑬
⑭6-1.40MIN
㉕22.50 0.00 −0.10 ▽
㉖24.00±0.10 ▽

SYMBOL	COMMON DIMENSIONS[1]			NOTE
	MIN[2]	NOM[2]	MAX[2]	
A	10.90	11.00	11.10	
A1	9.60	9.70	9.80	
A2	-	3.85	-	BASIC
A3	7.60	7.70	7.80	
A4	-	1.10	-	BASIC
A5	0.75	0.80	0.85	
A6	-	-	8.50	
A7	0.90	-	-	
A8	0.60	0.70	0.80	
A9	0.80	-	-	
B	14.90	15.00	15.10	
B1	6.30	6.40	6.50	
B2	1.64	1.84	2.04	
B3	1.30	1.50	1.70	
B4	0.42	0.52	0.62	
B5	2.80	2.90	3.00	
B6	5.50	-	-	
B7	0.20	0.30	0.40	
B8	1.00	1.10	1.20	
B9	-	-	9.00	
B10	7.80	7.90	8.00	
B11	1.10	1.20	1.30	
C	0.90	1.00	1.10	
C1	0.603	0.703	0.803	
C2	0.20	0.30	0.40	
C3	0.00	-	0.15	
D1	1.00	-	-	
D2	1.00	-	-	
D3	1.00	-	-	
R1	0.20	0.40	0.60	
R2	0.20	0.40	0.60	
R3	0.70	0.80	0.90	
R4	0.70	0.80	0.90	
R5	0.70	0.80	0.90	
R6	0.70	0.80	0.90	
R7	29.50	30.00	30.50	
R10	-	0.20	-	
R11	-	0.20	-	
R17	0.10	0.20	0.30	
R18	0.20	0.40	0.60	
R19	0.05	-	0.20	

Notes:

1. Dimensions are in millimeters
2. Dimensioning and tolerances are per ASME Y14.5M-1994.
3. Coplanarity is additive to C1 max thickness.