Approved	Design
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TOSHIBA SD Card Specification

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Application

This document describes the specifications of the Toshiba standard SDHC Card.

To commence the design of the host system for SDHC Card, please confirm the latest information and refer the 9.Host Interface design notes.

1. Production Code

Toshiba SDHC Card:

	Capacity	Model Name
SDHC Card	4GB	SD-M04G7B7 (VDC)
SDHC Card	4GB	SD-M04G7B7 (VDCCN)
SDHC Card	4GB	SD-M04G7B7K (VDC)
SDHC Card	8GB	SD-M08G7B7 (VDC)
SDHC Card	8GB	SD-M08G7B7 (VDCCN)
SDHC Card	8GB	SD-M08G7B7K (VDC)

Fig.1: SDHC Card Design

2. Product Overview

The SDHC Card is a Memory Card of Small and Thin with SDMI compliant Security method.

(SDMI: Secure Digital Music Initiative)

Contents in the Card can be protected by CPRM based security. This contents security can be accomplished by SDHC Card, host, and security application software combinations. This product is RoHS compatible.

3. SDHC Card Features

Table 1: SD card Features

Label Design, Contents, Media Format

Design	Toshiba Standard (Fig .1)	
Contents	None (OEM Design Available)	ID, MKB Programmed (Toshiba Specific)
Security Functions	SD Security Specification Ver.2.00 Compliant (CPRM Based) *CPRM: Contents Protection for Recording Media Specification	
Logical Format	SD File System Specification Ver.2.00 Compliant (DOS-FAT Based formatted)	

Physical, Electrical

Electrical	Operating Voltage: 2.7V to 3.6 V (Memory Operation) Interfaces: SD Card Interface, (SD: 4 or 1bit) SPI Mode Compatible SD Physical Layer Specification Ver.2.00 Compliant	
Physical	L: 32, W: 24, T: 2.1 (mm), Weight: 3g (Max) 2g (typ.) SD Physical Layer Specification Ver.2.00 Compliant (Detailed Dimensions attached: sheet. 1)	
Durability	SD Physical Layer Specification Ver.2.00 Compliant	
RoHS	RoHS Compatible	

Accessories

Guarantee	Not Applied (Available with OEM requirement)	
Description	Not Applied (Available with OEM requirement)	
Card Case	Not Applied (Available with OEM requirement)	
Card Label	Not Applied (Available with OEM requirement)	
Packaging	Not Applied (Available with OEM requirement) Refer to Appendix. 5-1 and 5-2.	

4. Compatibility

Compliant Specifications

- SD Memory Card Specifications
  - Compliant with PHYSICAL LAYER SPECIFICATION Ver.2.00. (Part1)
  - Compliant with FILE SYSTEM SPECIFICATION Ver.2.00. (Part2)
  - Compliant with SECURITY SPECIFICATION Ver.2.00. (Part3)

Supplementary Explanation are described in " 8.Others: Limited Conditions, SD Specification Compliance" in this document.

5. Physical Characteristics

5.1. Environmental Characteristics

1) Standard Operation Conditions

Absolute Maximum Temperature Range: Ta = -25 to +85 degrees centigrade
(Humidity less than RH = 95 %, Non condensed)

Recommended Operating Conditions: Ta = 0 to +55 degrees centigrade
(Humidity RH = 20% to 85 % Non condensed)

Note:
Absolute maximum temperature range shows the maximum range which can operate in some condition, and DOES NOT mean a guaranteed operation in any conditions.
For the Stable operations, the recommended operating conditions are suggested or please ask for the customized conditions to Toshiba sales representatives.

2) Storage Temperature

Absolute Maximum Temperature Range: Tstg = -40 to +85 degrees centigrade
(Humidity less than RH = 95% Non condensed)

Recommended Storage Conditions: Tstg = -20 to +65 degrees centigrade
(Humidity RH = 5% to 85% Non condensed)

Note:
Absolute maximum temperature range shows the maximum range to store.
However, DOES NOT mean a guaranteed conditions for long term.
There are some impacts on the SD card if stored in this temperature rage for long term.
For the long term storage period, the recommended storage conditions is suggested or please ask for the customized conditions to Toshiba sales representatives.

5.2. Physical Characteristics

Mechanical Write Protect Switch

A mechanical sliding tablet on the side of the card can use for write protect switch.
The host system shall be responsible for this function.

The card is in a “Write Protected” status when the tablet is located on the “Lock “ position.
The host system shall not write nor format the card in this status.

The card is in “Write Enabled” status when the tablet is moved to the opposite position (Un-Lock).
(Please refer the figures below for the tablet polarity.)

Please slide the tablet till the dead end (stopped position).
The tablet is set on the “Write Enabled” position when it is shipped.

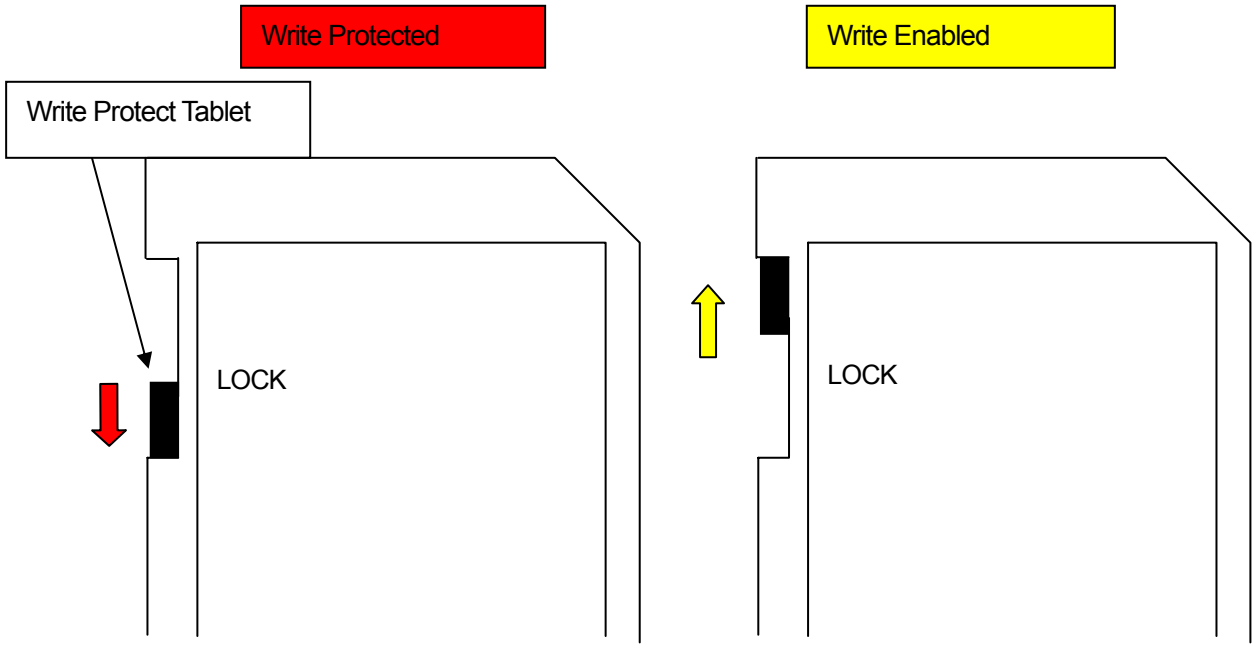

Fig 2: Write Protect Tablet Polarity (Front View)

6. Electrical Interface outlines

6.1. SD card pins

Table 2 describes the pin assignment of the SD card.
Fig.3 describes the pin assignment of the SD card.

Please refer the detail descriptions by SD Card Physical Layer Specification.

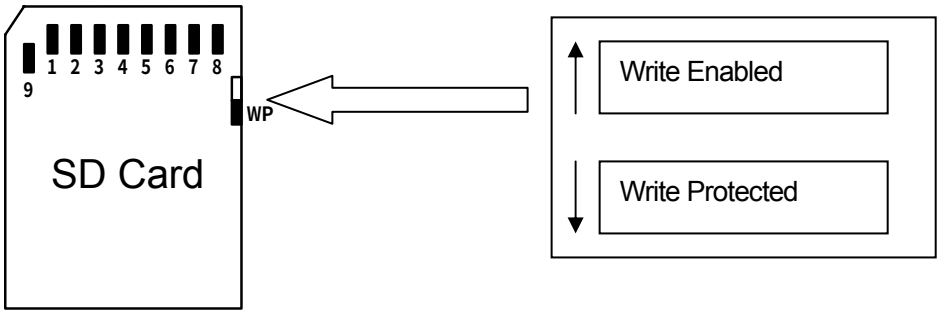

Fig3: SD Card Pin assignment (Back view of the Card)

Table 2:SD card pin assignment

Pins	SD Mode			SPI Mode		
	Name	IO type [1]	Description	Name	IO Type	Description
1	CD/ DAT3	I/O /PP	Card Detect/ Data Line [Bit3]	CS	I	Chip Select (Negative True)
2	CMD	PP	Command/Response	DI	I	Data In
3	V_{SS1}	S	Ground	V_{SS}	S	Ground
4	V_{dd}	S	Supply Voltage	V_{dd}	S	Supply Voltage
5	CLK	I	Clock	SCLK	I	Clock
6	V_{SS2}	S	Ground	V_{SS2}	S	Ground
7	DAT0	I/O /PP	Data Line [Bit0]	DO	O/PP	Data Out
8	DAT1	I/O /PP	Data Line [Bit1]	RSV	-	Reserved (*)
9	DAT2	I/O /PP	Data Line [Bit2]	RSV	-	Reserved (*)

1) S: Power Supply, I: Input, O: Output, I/O: Bi-directionally,'PP' - IO using push-pull drivers
(*) These signals should be pulled up by host side with 10-100k ohm resistance in the SPI Mode.

6.2 SD Card Bus Topology

The SD Memory Card supports two alternative communication protocols: SD and SPI Bus Mode.

Host System can choose either one of modes. Same Data of the SDHC Card can read and write by both modes.

SD Mode allows the 4-bit high performance data transfer. SPI Mode allows easy and common interface for SPI channel.
The disadvantage of this mode is loss of performance, relatively to the SD mode.

6.2.1 SD Bus Mode protocol

The SD bus allows the dynamic configuration of the number of data line from 1 to 4 Bi-directional data signal.
After power up by default, the SD card will use only DAT0. After initialization, host can change the bus width.

Multiplied SD cards connections are available to the host. Common V_{dd}, V_{ss} and CLK signal connections are available in the multiple connections. However, Command, Respond and Data lined (DAT0-DAT3) shall be divided for each card from host.
This feature allows easy trade off between hardware cost and system performance. Communication over the SD bus is based on command and data bit stream initiated by a start bit and terminated by stop bit.

Command:
Commands are transferred serially on the CMD line. A command is a token to starts an operation from host to the card. Commands are sent to an addressed single card (addressed Command) or to all connected cards (Broad cast command).

Response:
Responses are transferred serially on the CMD line.
A response is a token to answer to a previous received command. Responses are sent from an addressed single card or from all connected cards.

Data:
Data can be transfer from the card to the host or vice versa.
Data is transferred via the data lines.

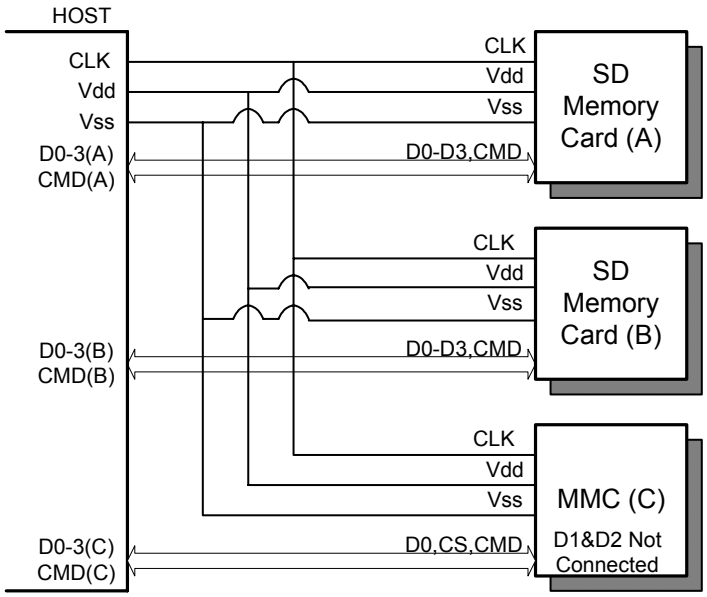

Fig 4: SD Card (SD Mode) connection Diagram

CLK:	Host card Clock signal
CMD:	Bi-directional Command/ Response Signal
DAT0 - DAT3:	4 Bi-directional data signal
V_{dd}:	Power supply
V_{ss}:	GND

Table 3: SD Mode Command Set

(+: Implemented, -: Not Implemented)

CMD Index	Abbreviation	Implementation	Note
CMD0	GO_IDLE_STATE	+	
CMD2	ALL_SEND_CID	+	
CMD3	SEND_RELATIVE_ADDR	+	
CMD4	SET_DSR	-	DSR Register is not implemented.
CMD6	SWITCH_FUNC	+	
CMD7	SELECT/DESELECT_CARD	+	
CMD9	SEND_CSD	+	
CMD10	SEND_CID	+	
CMD12	STOP_TRANSMISSION	+	
CMD13	SEND_STATUS	+	
CMD15	GO_INACTIVE_STATE	+	
CMD16	SET_BLOCKLEN	+	
CMD17	READ_SINGLE_BLOCK	+	
CMD18	READ_MULTIPLE_BLOCK	+	
CMD24	WRITE_BLOCK	+	
CMD25	WRITE_MULTIPLE_BLOCK	+	
CMD27	PROGRAM_CSD	+	
CMD28	SET_WRITE_PROT	-	Internal Write Protection is not implemented.
CMD29	CLR_WRITE_PROT	-	Internal Write Protection is not implemented.
CMD30	SEND_WRITE_PROT	-	Internal Write Protection is not implemented.
CMD32	ERASE_WR_BLK_START	+	
CMD33	ERASE_WR_BLK_END	+	
CMD38	ERASE	+	
CMD42	LOCK_UNLOCK	+	
CMD55	APP_CMD	+	
CMD56	GEN_CMD	-	This command is not specified.
ACMD6	SET_BUS_WIDTH	+	
ACMD13	SD_STATUS	+	
ACMD22	SEND_NUM_WR_BLOCKS	+	
ACMD23	SET_WR_BLK_ERASE_COUNT	+	
ACMD41	SD_APP_OP_COND	+	
ACMD42	SET_CLR_CARD_DETECT	+	
ACMD51	SEND_SCR	+	
ACMD18	SECURE_READ_MULTI_BLOCK	+	
ACMD25	SECURE_WRITE_MULTI_BLOCK	+	
ACMD26	SECURE_WRITE_MKB	+	
ACMD38	SECURE_ERASE	+	
ACMD43	GET_MKB	+	
ACMD44	GET_MID	+	
ACMD45	SET_CER_RN1	+	
ACMD46	SET_CER_RN2	+	
ACMD47	SET_CER_RES2	+	
ACMD48	SET_CER_RES1	+	
ACMD49	CHANGE_SECURE_AREA	+	

- CMD28, 29 and CMD30 are Optional Commands.
- CMD4 is not implemented because DSR register (Optional Register) is not implemented.
- CMD56 is for vender specific command. Which is not defined in the standard card.

6.2.2 SPI Bus mode Protocol

The SPI bus allows 1 bit Data line by 2-chanel (Data In and Out).

The SPI compatible mode allows the MMC Host systems to use SD card with little change.
The SPI bus mode protocol is byte transfers.

All the data token are multiples of the bytes (8-bit) and always byte aligned to the CS signal.

The advantage of the SPI mode is reducing the host design in effort.

Especially, MMC host can be modified with little change.

The disadvantage of the SPI mode is the loss of performance versus SD mode.

Caution: Please use SD Card Specification. DO NOT use MMC Specification.

For example, initialization is achieved by ACMD41, and be careful to Register. Register definition is different, especially CSD Register.

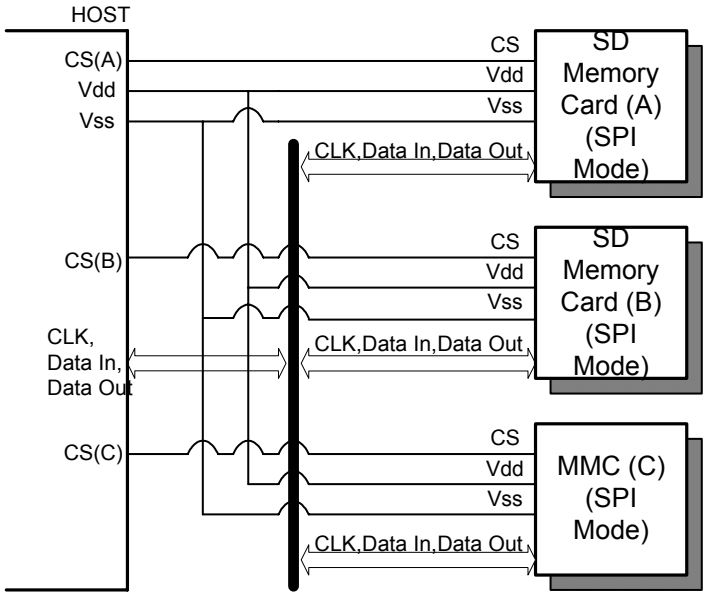

Fig 5: SD card (SPI mode) connection diagram

CS:	Card Select Signal
CLK:	Host card Clock signal
Data in:	Host to card data line
Data out:	card to host data line
V_{dd}:	Power supply
V_{ss}:	GND

Table.4: SPI Mode Command set
(+: Implemented, -: Not Implemented)

CMD Index	Abbreviation	Implementation	Note
CMD0	GO_IDLE_STATE	+	
CMD1	SEND_OP_CND	+	NOTICE: DO NOT USE (SEE Fig.6 and 9.2)
CMD6	SWITCH_FUNC	+	
CMD9	SEND_CSD	+	
CMD10	SEND_CID	+	
CMD12	STOP_TRANSMISSION	+	
CMD13	SEND_STATUS	+	
CMD16	SET_BLOCKLEN	+	
CMD17	READ_SINGLE_BLOCK	+	
CMD18	READ_MULTIPLE_BLOCK	+	
CMD24	WRITE_BLOCK	+	
CMD25	WRITE_MULTIPLE_BLOCK	+	
CMD27	PROGRAM_CSD	+	
CMD28	SET_WRITE_PROT	-	Internal Write Protection is not implemented.
CMD29	CLR_WRITE_PROT	-	Internal Write Protection is not implemented.
CMD30	SEND_WRITE_PROT	-	Internal Write Protection is not implemented.
CMD32	ERASE_WR_BLK_START_ADDR	+	
CMD33	ERASE_WR_BLK_END_ADDR	+	
CMD38	ERASE	+	
CMD42	LOCK_UNLOCK	+	
CMD55	APP_CMD	+	
CMD56	GEN_CMD	-	This command is not specified.
CMD58	READ_OCR	+	
CMD59	CRC_ON_OFF	+	
ACMD6	SET_BUS_WIDTH	+	
ACMD13	SD_STATUS	+	
ACMD22	SEND_NUM_WR_BLOCKS	+	
ACMD23	SET_WR_BLK_ERASE_COUNT	+	
ACMD41	SD_APP_OP_COND	+	
ACMD42	SET_CLR_CARD_DETECT	+	
ACMD51	SEND_SCR	+	
ACMD18	SECURE_READ_MULTI_BLOCK	+	
ACMD25	SECURE_WRITE_MULTI_BLOCK	+	
ACMD26	SECURE_WRITE_MKB	+	
ACMD38	SECURE_ERASE	+	
ACMD43	GET_MKB	+	
ACMD44	GET_MID	+	
ACMD45	SET_CER_RN1	+	
ACMD46	SET_CER_RN2	+	
ACMD47	SET_CER_RES2	+	
ACMD48	SET_CER_RES1	+	
ACMD49	CHANGE_SECURE_AREA	+	

- CMD28, 29 and CMD30 are Optional Commends.
- CMD56 is for vender specific command. Which is not defined in the standard card.

6.3. Card Initialize

To initialize the Toshiba SD card, follow the following procedure is recommended example.

1) Supply Voltage for initialization.

Host System can apply the Operating Voltage from initialization to the card.

Apply more than 74 cycles of Dummy-clock to the SD card.

2) Select operation mode (SD mode or SPI mode)

In case of SPI mode operation, host should drive 1 pin (CD/DAT3) of SD Card I/F to “Low” level. Then, issue CMD0.

In case of SD mode operation, host should drive or detect 1 pin of SD Card I/F (Pull up register of 1 pin is pull up to “High” normally).

Card maintain selected operation mode except re-issue of CMD0 or power on below is SD mode initialization procedure.

3) Send the ACMD41 with Arg = 0 and identify the operating voltage range of the Card.
4) Apply the indicated operating voltage to the card.

Reissue ACMD41 with apply voltage storing and repeat ACMD41 until the busy bit is cleared.

(Bit 31 Busy = 1) If response time out occurred, host can recognize not SD Card.

Note: In MMC-SPI Mode, CMD1 can use in this state.
However, do not use CMD1 in case of SD Mode.

5) Issue the CMD2 and get the Card ID (CID).

Issue the CMD3 and get the RCA. (RCA value is randomly changed by access, not equal zero)

6) Issue the CMD7 and move to the transfer state.

If necessary, Host may issue the ACMD42 and disabled the pull up resistor for Card detect.

7) Issue the ACMD13 and poll the Card status as SD Memory Card. Check SD_CARD_TYPE value. If significant 8 bits are “all zero”, that means SD Card. If it is not, stop initialization.

8) Issue CMD7 and move to standby state.

Issue CMD9 and get CSD.

Issue CMD10 and get CID.

9) Back to the Transfer state with CMD7.

Issue ACMD6 and choose the appropriate bus-width.

Then the Host can access the Data between the SD card as a storage device.

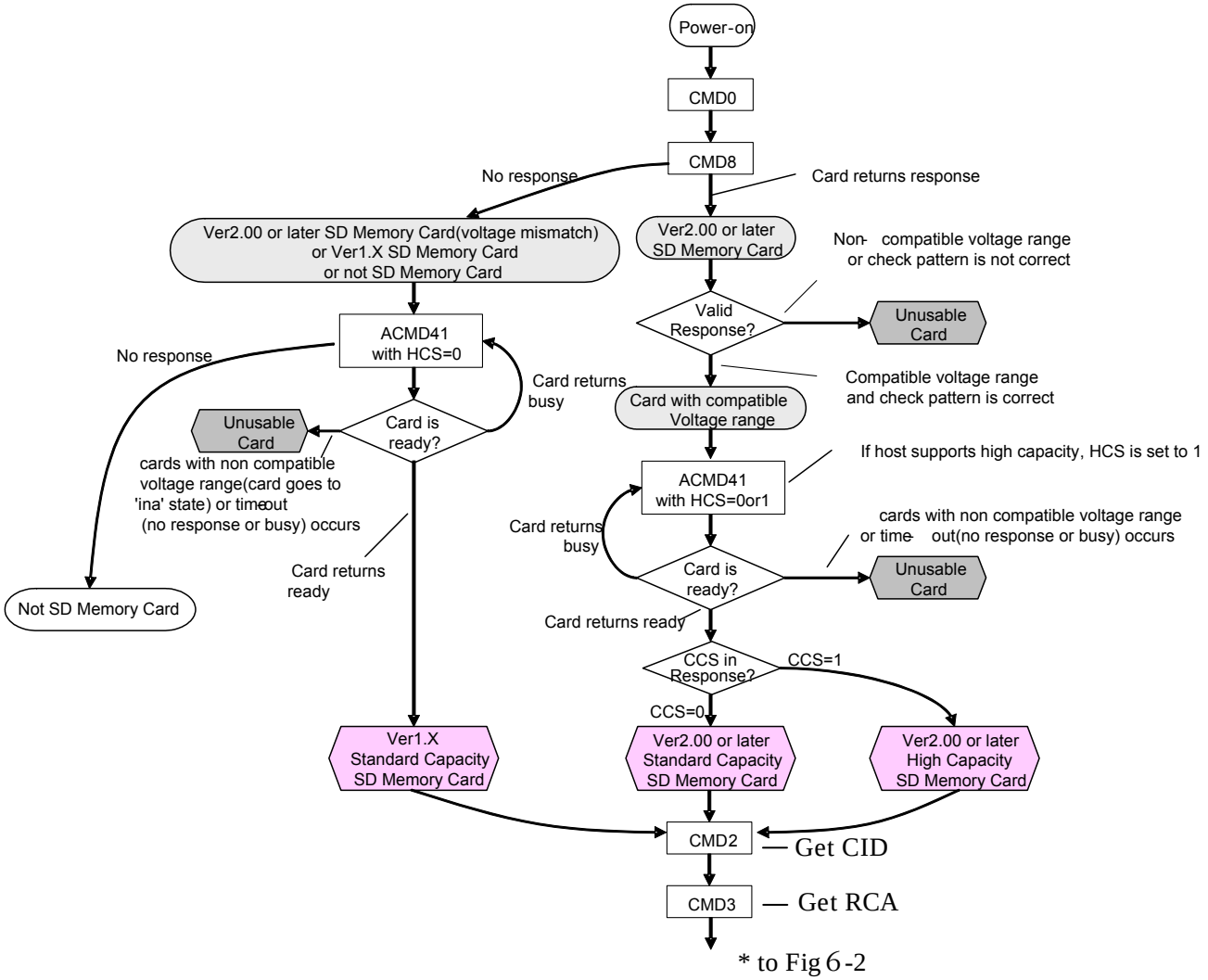

Fig 6-1. SD card Initialize Procedure

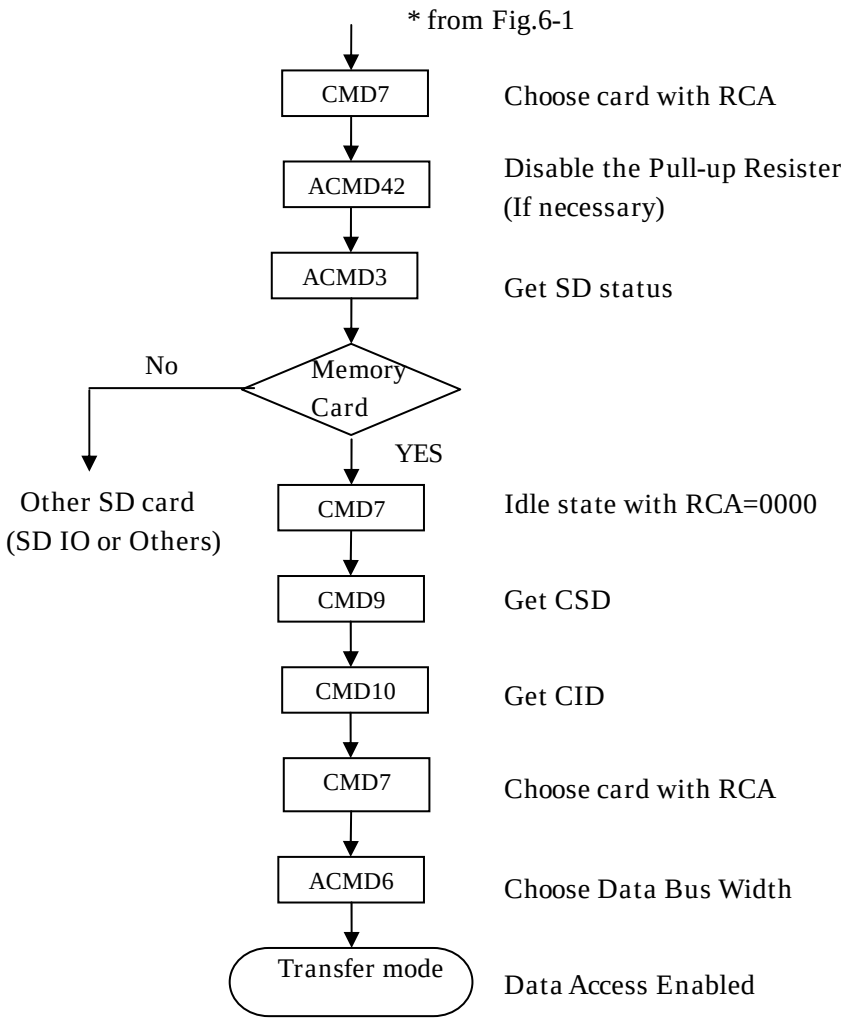

Fig 6-2. SD card Initialize Procedure

6.4. SD card Electrical Characteristics

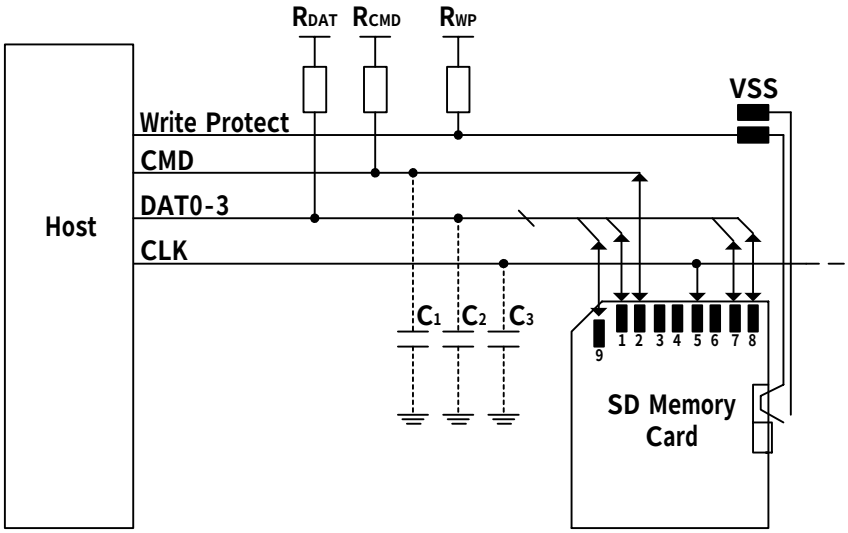

Fig7: SD card Connection diagram

6.4.1 Absolute Maximum Conditions

Table 5: Absolute Maximum Conditions

Item	Symbol	Value	Unit
Supply Voltage	V_{DD}	-0.3 to 4.6	V
Input Voltage	V_{IN}	-0.3 to VDD+0.3	V

6.4.2 DC Characteristics

Table 6: DC Characteristics

Item		Symbol	Condition	MIN.	Typ.	MAX.	Unit	Note
Supply Voltage 1		V_{DD}	-	2.0	-	3.6	V	For CMD0, 15,55, ACMD41 Only
Supply Voltage 2			-	2.7	-	3.6	V	For All commands
Input Voltage	High Level	V_{IH}	-	VDD*0.625	-	-	V	
	Low Level	V_{IL}	-	-	-	VDD*0.25	V	
Output Voltage	High Level	V_{OH}	VDD = 2V IOH = -100uA	VDD*0.75	-	-	V	
	Low Level	V_{OL}	VDD = 2V IOL = 100uA	-	-	VDD*0.125	V	
Standby Current		I_{CC1}	3.6V Clock 25MHz	-	-	30	mA	
			3.0V Clock Stop	-	-	0.25		@25 deg C
Operation Current *)		I_{CC2}	3.6V/25MHz, 50MHz	-	-	150	mA	Write
				-	-	150		Read
Input Voltage Setup Time		Vrs	-	-	-	250	ms	

*) Peak Current: RMS value over a 10usec period

Table 7: Signal Capacitance

Item	Symbol	Min.	Max.	Unit	Note
Pull up Resistance	R_{CMD} R_{DAT}	10	100	K Ohm	
Bus Signal Line Capacitance	C_L	-	250	pF	F_{PP}<5MHz (21Cards)
Bus Signal Line Capacitance	C_L	-	100	pF	F_{PP}<20MHz (7Cards)
Single Card Capacitance	C_{CARD}	-	10	pF	
Pull up Resistance inside card(pin1)	R_{DAT3}	10	90	K Ohm	

Note: WP pull-up (R_{wp}) Value is depend on the Host Interface drive circuit.

6.4.3 AC Characteristics (Default)

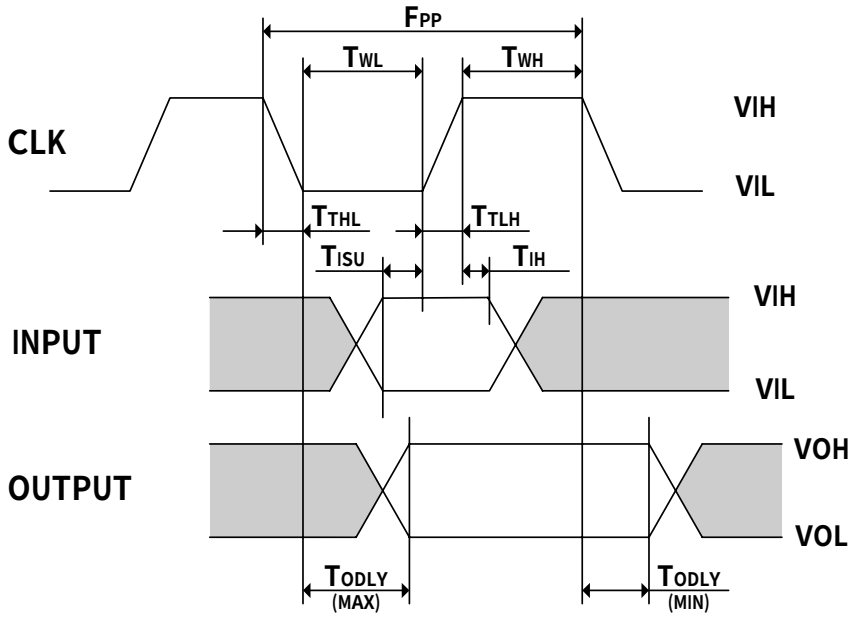

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Fig 8-1: AC Timing Diagram (Default)

Table 8-1: AC Characteristics (Default)

Item	Symbol	Min.	Max.	Unit	Note
Clock Frequency (In any Sates)	F_{sty}	0	25	MHz	C_L<100pF (7Cards)
Clock Frequency (Data transfer Mode)	F_{PP}	0.1	25	MHz	C_L<100pF (7Cards)
Clock Frequency (Card identification Mode)	F_{OD}	100	400	kHz	C_L<250pF (21Cards)
Clock Low Time	T_{WL}	10	-	ns	C_L<100pF (7Cards)
Clock High Time	T_{WH}	10	-	ns	
Clock Rise Time	T_{TLH}	-	10	ns	
Clock Fall Time	T_{THL}	-	10	ns	
Clock Low Time	T_{WL}	50	-	ns	C_L < 250pF (21Cards)
Clock High Time	T_{WH}	50	-	ns	
Clock Rise Time	T_{TLH}	-	50	ns	
Clock Fall Time	T_{THL}	-	50	ns	
Input Setup Time	T_{ISU}	5	-	ns	C_L < 25pF (1Cards)
Input Hold Time	T_{IH}	5	-	ns	
Output Delay Time	T_{ODLY}	0	14	ns	

6.4.4 AC Characteristics (High-Speed)

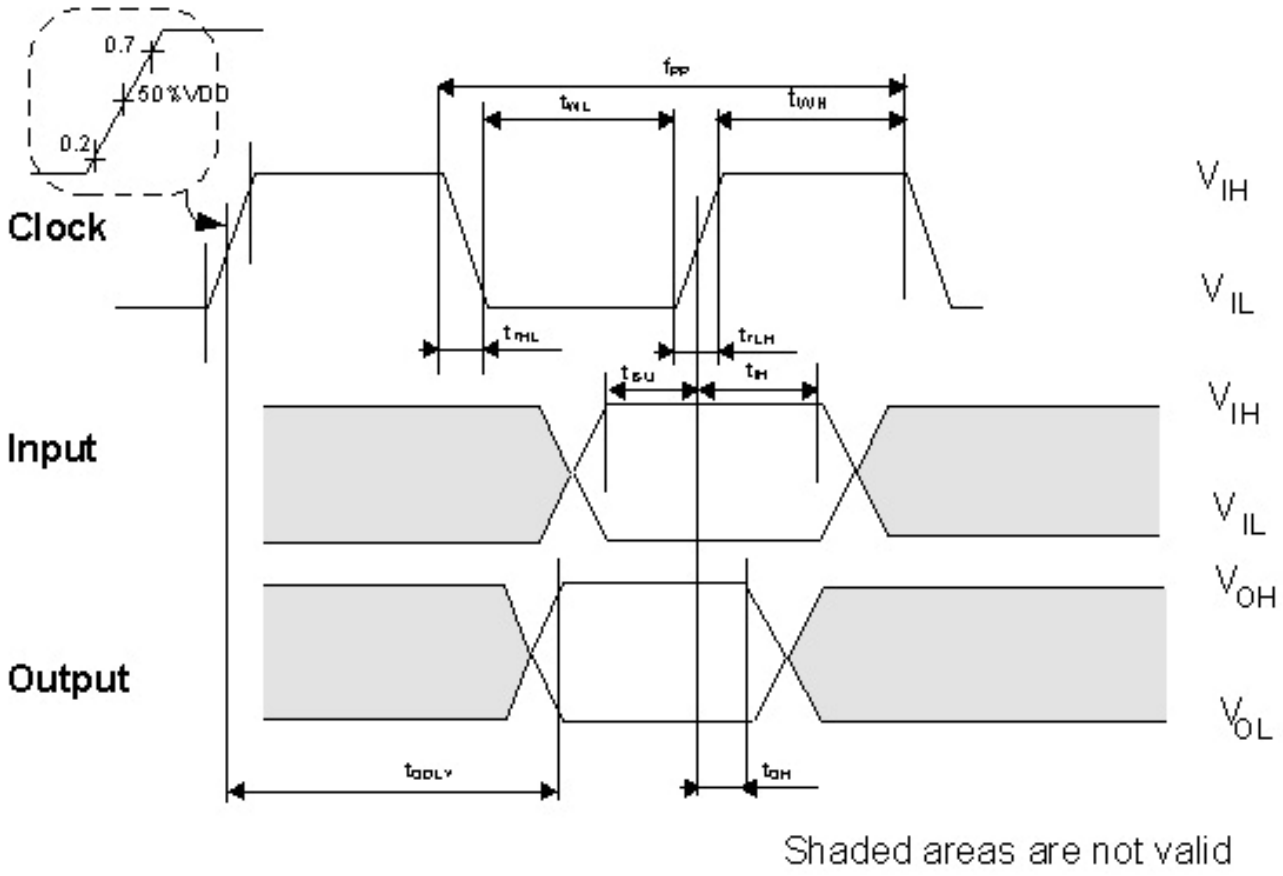


Fig 8-2: AC Timing Diagram (High-Speed)

Table 8-2: AC Characteristics (High-Speed)

Item	Symbol	Min.	Max.	Unit	Note
Clock Frequency (During Data transfer)	f_{PP}	0	50	MHz	
Clock Low Time	t_{WL}	7	—	ns	
Clock High Time	t_{WH}	7	—	ns	
Clock Rise Time	t_{TLH}	—	3	ns	
Clock Fall Time	t_{THL}	—	3	ns	
Input Setup Time	t_{ISU}	6	—	ns	
Input Hold Time	t_{IH}	2	—	ns	
Output Delay Time	T_{ODLY}	0	14	ns	
Output Hold Time	T_{OH}	2.5	-	ns	
Total System capacitance for each line	C_L	-	40	pF	

7. Card Internal Information

7.1. Security Information

MKB (Media Key Block) and Media ID are Toshiba Standard Information. These informations are compliance with the CPRM.
Note: The security information is NOT Development information for evaluation.
Host System shall be compliance with the CPRM to use the security function.
This information is kept as confidential because of security reasons.

7.2. SD Card Registers

The SD card has six registers and SD Status information: OCR, CID, CSD, RCA, DSR, SCR and SD Status.
DSR IS NOT SUPPORTED in this card.

There are two types of register groups.

MMC compatible registers: OCR, CID, CSD, RCA, DSR, and SCR
SD card Specific: SD Status

Table.9: SD card Registers

Resister Name	Bit Width	Description
OCR	32	Operation Conditions (VDU Voltage Profile and Busy Status Information)
CID	128	Card Identification information
CSD	128	Card specific information
RCA	16	Relative Card Address
DSR	16	Not Implemented (Programmable Card Driver): Driver Stage Register
SCR	64	SD Memory Card's special features
SD Status	512	Status bits and Card features

7.2.1. OCR Register

This 32-bit register describes operating voltage range and status bit in the power supply.
(Refer Appendix 2. for the detail)

Table.10: OCR register definition

OCR bit position	VDD voltage window	Initial value		
		4GB	8GB	
31	Card power up status bit (busy)	"0" = busy "1" = ready		
30	Card Capacity Status	"0"=SD Memory Card "1"=SDHC Memory Card		
29-24	reserved	All '0'		
23	3.6 – 3.5	1		
22	3.5 – 3.4	1		
21	3.4 – 3.3	1		
20	3.3 – 3.2	1		
19	3.2 – 3.1	1		
18	3.1 – 3.0	1		
17	3.0 – 2.9	1		
16	2.9 – 2.8	1		
15	2.8 – 2.7	1		
14	2.7 – 2.6	0		
13	2.6 – 2.5	0		
12	2.5 – 2.4	0		
11	2.4 – 2.3	0		
10	2.3 – 2.2	0		
9	2.2 – 2.1	0		
8	2.1 – 2.0	0		
7	2.0 – 1.9	0		
6	1.9 – 1.8	0		
5	1.8 – 1.7	0		
4	1.7 – 1.6	0		
3-0	reserved	All '0'		

bit 23-4: Describes the SD Card Voltage
bit 31 indicates the card power up status. Value "1" is set after power up and initialization procedure has been completed.

7.2.2. CID Register

The CID (Card Identification) register is 128-bit width. It contains the card identification information.
(Refer Appendix 3. for the detail) The Value of CID Register is vender specific.

Tabel.11: CID Register

Field	Width	CID-slice	Initial Value		
			4GB	8GB	
MID	8	[127:120]	02 h		
OID	16	[119:104]	"TM" (544D h)		
PNM	40	[103:64]	"SD04G"	"SD08G"	
PRV	8	[63:56]	(a) Product revision		
PSN	32	[55:24]	(a) Product serial number		
-	4	[23:20]	All '0'		
MDT	12	[19:8]	(b) Manufacture date		
CRC	7	[7:1]	(c) CRC		
-	1	[0:0]	1		

(a), (b): Depends on the SD Card. Controlled by Production Lot.
(c) Depends on the CID Register

• MID

8 bit binary number, Indicates the Manufacture ID allocated by the SDA.
→02 -h (Indicates Toshiba) (Unit: -h means Hex-decimal value, here after)

• OID

16 bit binary number, Indicates the Manufacture ID allocated by the SDA.
→544D -h = "TM" in ASCII String (Indicates Toshiba)

• PNM

5 ASCII Characters long (40 bit), Toshiba Product Code.
→ Toshiba Standard SD card indicates as below by capacity.
4GB: "SD04G" (0x5344303447)
8GB: "SD08G" (0x5344303847)

• PRV

Product Revision of the card.
→ Currently 00 -h = Rev.0. 0:This number may be changed without any notice by TOSHIBA.

• PSN

32 bit serial number of unsigned integer.
→ Uniquely assigned integer

• MDT

The manufacturing date composed of two-hexadecimal digits.
→ CID-Slice [11:8] Month Field (Exp. 1h = January)
CID-Slice [19:12] Year Field (Exp. 0h = 2000)

• CRC

Checksum of CID contents.
→ CRC 7 Checksum (See Chapter 7. of the SD PHYSICAL SPECIFICATION)

7.2.3. CSD Register

CSD is Card-Specific Data register provides information on 128bit width.
Some field of this register can writable by PROGRAM_CSD (CMD27).

Table.12: CSD Register

				Initial Value		
Field	Width	Cell Type(1)	CSD slice	4GB	8GB	
CSD_STRUCTURE	2	R	[127:126]	01		
-	6	R	[125:120]	All '0'		
TAAC	8	R	[119:112]	0_0001_110(1ms)		
NSAC	8	R	[111:104]	00000000		
TRAN_SPEED	8	R	[103:96]	0_0110_010(25Mbps)		
CCC	12	R	[95:84]	0_1_0_1_1_0_1_1_0_1_0_1		
READ_BL_LEN	4	R	[83:80]	1001	1001	
READ_BL_PARTIAL	1	R	[79:79]	0		
WRITE_BLK_MISALIGN	1	R	[78:78]	0		
READ_BLK_MISALIGN	1	R	[77:77]	0		
DSR_IMP	1	R	[76:76]	0		
-	6	R	[75:70]	All '0'		
C_SIZE	22	R	[69:48]	0x1DFF	0x3BFF	
-	1	R	[47:47]	0		
ERASE_BLK_EN	1	R	[46:46]	1		
SECTOR_SIZE	7	R	[45:39]	11_1111_1		
WP_GRP_SIZE	7	R	[38:32]	000_0000		
WP_GRP_ENABLE	1	R	[31:31]	0		
-	2	R	[30:29]	00		
R2W_FACTOR	3	R	[28:26]	010		
WRITE_BL_LEN	4	R	[25:22]	1001		
WRITE_BL_PARTIAL	1	R	[21:21]	0		
-	2	R	[20:16]	All '0'		
FILE_FORMAT_GRP	1	R	[15:15]	0		
COPY	1	R/W(1)	[14:14]	0		
PERM_WRITE_PROTECT	1	R/W(1)	[13:13]	0		
TMP_WRITE_PROTECT	1	R/W	[12:12]	0		
FILE_FORMAT	2	R	[11:10]	00		
-	2	R	[9:8]	All '0'		
CRC	7	R/W	[7:1]	(CRC)		
-	1	-	[0:0]	1		

Cell Types: R: Read Only, R/W: Writable and Readable, R/W(1): One-time Writable / Readable
Note: Erase of one data block is not allowed in this card. This information is indicated by "ERASE_BLK_EN".
Host System should refer this value before one data block size erase.

・CSD_STRUCTURE

Version number of the related CSD structure.

Table 12-1:CSD_STRUCTURE

CSD_STRUCTURE	CSD STRUCTURE VERSION	Valid for SD PHYSICAL LAYER SPECIFICATION Version
0	CSD Version 1.0	Version 1.0-1.10 Version 2.00/Standard Capacity
1	CSD Version 2.0	Version 2.00/High Capacity
2-3	Reserved	

→ Version 2.0 Compliant

・TAAC

Defines the asynchronous part of the data access time.

Table 12-2: TAAC Access Time Definition

TAAC bit	Code
2:0	Time Unit 0 = 1ns,1 = 10ns,2 = 100ns,3 = 1*u*S,4 = 10*u*S,5 = 100*u*S, 6 = 1ms,y = 10ms
6:3	Time Value 0 = Reserved,1 = 1.0,2 = 1.2,3 = 1.3,4 = 1.5,5 = 2.0, 6 = 2.5, 7 = 3.0,8 = 3.5,9 = 4.0,A = 4.5,B = 5.0,C = 5.5,D = 6.0, E = 7.0,F = 8.0
7	Reserved

→1ms

・NSAC

Defines the worst case for the clock dependent factor of the data access time.

Unit is 100 clock cycle.

Total access time equal TAAC plus NSAC, calculation with actual clock frequency.

This is average delay by the first clock out put for data block.

→0 clock Cycle

・TRAN_SPEED

The following table defines the maximum data transfer rate per one data line.

Table 12-3: Maximum Data Transfer Rate Definition

TRAN_SPEED bit	Code
2:0	Transfer Rate Unit 0 = 100kbit/s,1 = 1Mbit/s,2 = 10Mbit/s,3 = 100Mbit/s, 4-7 = Reserved
6:3	Time Value 0 = Reserved,1 = 1.0,2 = 1.2,3 = 1.3,4 = 1.5,5 = 2.0, 6 = 2.5, 7 = 3.0,8 = 3.5,9 = 4.0,A = 4.5,B = 5.0,C = 5.5,D = 6.0, E = 7.0,F = 8.0
7	Reserved

→ Trans Rate is 25Mbps

・CCC

The Card Class Command Register (CCC) defines which command classes are supported by this card.

Table12-4: Supported Card Command Classes

CCC bit	Supported Card command Class
0	Class 0
1	Class 1
...	
11	Class 11

→ Class 0,2,4,5,7,8 ,10 are supported

・READ_BL_LEN

The Maximum read data block length for reading is computed as $2^{READ\_BL\_LEN}$.
READ_BL_LEN is always equal to WRITE_BL_LEN.

Table12-5:DATA Block Length

READ_BL_LEN	Block Length
0-8	Reserved
9	2^9 = 512Bytes
・・・	
11	2^{11} = 2048Bytes
12-15	Reserved

→512Bytes

・READ_BL_PARTIAL

This field is fixed “0”.

→”0”: Partial block read is inhibited and only unit of block access is allowed.

・WRITE_BLK_MISALIGN

Define whether the data block to be written by one command can be spread over more than one physical block of the Flash Memory Device.

Table 12-6:WRITE_BLK_MISALIGN

WRITE_BLK_MISALIGN	Across Block Boundaries Write
0	Not Allowed
1	Allowed

→”0”: Not allowed on this card

・READ_BLK_MISALIGN

Define whether the data block to be read by one command can be spread over more than one physical block of the Flash Memory Device.

Table 12-7: READ_BLK_MISALIGN

READ_BLK_MISALIGN	Across Block Boundaries Read
0	Not Allowed
1	Allowed

→"0": Invalid on this card

・DSR_IMP

If set, a driver stage register (DSR) is implemented (supported).

Table 12-8: DSR_IMP

DSR_IMP	DSR Type
0	DSR NOT Implemented
1	DSR Implemented

→"0": DSR NOT implemented

・C_SIZE

This parameter is used to compute the user's data card capacity(Not include the security area) as below.

Memory Capacity = BLOCKNR * BLOCK_LEN

BLOCKNR = (C_SIZE + 1) * 512 KB

→ The user's data card capacity is as below.
4GB: 3840 MB
8GB: 7680 MB

・ERASE_BLK_EN

(Caution!: This is different from MMC. Please be careful.)

WRITE_BL_LEN defines whether erase of one write block(see WRITE_BL_LEN) is allowed.

Table12-12: ERASE_BLK_EN

ERASE_BLK_EN	Description
0	Host cannot erase by WRITE_BL_LEN
1	Host can erase by WRITE_BL_LEN

→"1" : Can erase by WRITE_BL_LEN unit (512 Bytes)
So should be check this value, and recognize how to erase.

・SECTOR_SIZE

This field is fixed to “11_1111_1”. This value does not relate to erase operation. On this cards memory boundary is indicated by AU size and this field should not be used.

・WP_GRP_SIZE

This field is fixed “0x00”. The high capacity SD Memory card does not support write protected groups.

・WP_GRP_ENABLE

This field is fixed “0”. The high capacity SD Memory card does not support write protected groups.

Table12-13: WP_GRP_ENABLE

WP_GRP_ENABLE	Description
0	NOT Implemented
1	Implemented

→”0”: WP Group is not Implemented on this card

・R2W_FACTOR

This field is fixed to “0x2”, which indicates 4 multiples. However, host should not use this factor and should use 250ms for write timeout.

Table12-14: R2W_FACTOR

R2W_FACTOR	Multiples of read Access Time
0	1
1	2(Write half as fast as read)
2	4
3	8
4	16
5	32
6,7	Reserved

・WRITE_BL_LEN

The maximum write block length is calculated as $2^{WRITE\_BL\_LEN}$.

Table12-15: DATA Block Length

WRITE_BL_LEN	Block Length
0-8	Reserved
9	2^9 = 512Bytes
・・・	
11	2^{11} = 2048Bytes
12-15	Reserved

→"9": 512Bytes,on this card

・WRITE_BL_PARTIAL

This field is fixed to "0", which indicates partial block is inhibited and only unit of block access is allowed.

Table12-16: Write Data size

WRITE_BL_PARTIAL	Block Oriented write Data size
0	Only the WRITE_BL_LEN size or 512Bytes are available
1	Partial size (Minimum 1Byte) write available

→"0": Partial size write is not available on this card

・FILE_FORMAT_GRP

This field is set to "0". Host should not use this field.

・COPY

Defines the contents of this card is original (=0) or duplicated (1).
This bit is one time programmable.

Table12-18: COPY

COPY	Description
0	Original
1	Copy

→"0": Original on this card

・PERM_WRITE_PROTECT

Permanently protects the whole card content against write or erase.
This bit is one time programmable.

Table12-19: PERM_WRITE_PROTECT

PERM_WRITE_PROTECT	Description
0	Not protected/Writable
1	Permanently Write protected

→"0": Not Protected/Writable on this card

・TMP_WRITE_PROTECT

Temporarily protects the whole card content against write or erase.

Table12-20: TMP_WRITE_PROTECT

TMP_WRITE_PROTECT	Description
0	Not protected/Writable
1	Temporarily Write Erase protected

→"0": Not Protected/Writable on this card

・FILE_FORMAT

This field is set to "0". Host should not use this field.

Table12-17: File Format

FILE_FORMAT	Kinds
0	Hard disk-like File system with partition table
1	DOS FAT(floppy-like) with boot sector only (No partition table)
2	Universal File Format
3	Others/Unknown
0,1,2,3	Reserved

・CRC

Calculated CRC for default data is set here.
Host System is responsible to re-calculate this CRC if any CSD contents are changed.

7.2.4. RCA Register

The writable 16bit relative card address register carries the card address in SD Card mode.

7.2.5. DSR Register

This register is not implemented on this card

7.2.6. SCR Register

SCR (SD Card Configuration Register) provides information on SD Memory Card's special features.
The size of SCR Register is 64 bit.

Table13: SCR Register

Field	Width	Cell Type	SCR Slice	Value		
				4GB	8GB	
SCR_STRUCTURE	4	R	[63:60]	0000		
SD_SPEC	4	R	[59:56]	0010		
DATA_STAT_AFTER_ERASE	1	R	[55:55]	1		
SD_SECURITY	3	R	[54:52]	011		
SD_BUS_WIDTHS	4	R	[51:48]	0101		
-	16	R	[47:32]	All '0'		
-	32	R	[31:0]	Reserved for manufacture usage		

・SCR_STRUCTURE

Version number of the related structure in the SD Card PHYSICAL LAYER SPECIFICATION.

Table13-1: SCR_STRUCTURE

SCR_STRUCTURE	SCR STRUCTURE VERSION	Valid for SD PHYSICAL LAYER SPECIFICATION
0	SCR Version 1.0	Version 1.0-2.00
1-15	Reserved	

→"0": Version 1.0 Compliant on this card

・SD_SPEC

Describes the SD PHYSICAL LAYER SPECIFICATION version supported by this card.

Table13-2: SD_SPEC

SD_SPEC	SD PHYSICAL LAYER SPECIFICATION Version
0	Version 1.0-1.01
1	Version 1.10
2	Version2.00
3-15	Reserved

→"2" = Version2.00 Compliant on this card

・DATA_STAT_AFTER_ERASE

This indicates the block “0” or “1” after erase operation.

→”1” on this card

・SD_SECURITY

Describe the security algorithm supported by the Card.

Table13-3: Supported Security Algorithm

SD_SECURITY	Supported Security Specification
0	No Security
1	Not used
2	Version 1.01
3	Version 2.0
4-7	Reserved

→”3”: Version 2.0 on this card

・SD_BUS_WIDTHS

Indicates the DAT bus width that a supported by this card.

Table 13-4:Supported Bus Widths

SD_BUS_WIDTHS	Supported BUS width
0 bit position	1 bit(DAT0)
1st bit position	Reserved
2nd bit position	4 bit(DAT0-3)
3rd bit position	Reserved

→”0101”: 1 and 4 bit supported.

7.2.7. SD Status

Table14: SD Status

Identifier	Width	Type	SD Status Slice	Value		
				4GB	8GB	
DAT_BUS_WIDTH	2	SR	[511:510]	0x0000		
SECURED_MODE	1	SR	[509]	0		
-	13	-	[508:496]	All '0'		
SD_CARD_TYPE	16	SR	[495:480]	0x0000		
SIZE_OF_PROTECTED_AREA	32	SR	[479:448]	0x02000000	0x03000000	
SPEED_CLASS	8	SR	[447:440]	0x02		
PERFORMANCE_MOVE	8	SR	[439:432]	0x02		
AU_SIZE	4	SR	[431:428]	0x9		
-	4	-	[427:424]	All '0'		
ERASE_SIZE	16	SR	[423:408]	0x0200	0x0200	
ERASE_TIMEOUT	6	SR	[407:402]	42	42	
ERASE_OFFSET	2	SR	[401:400]	2		
-	88	-	[399:312]	All '0'		
-	312	-	[311:0]	Reserved for manufacturer		

S: Status bit

R: Set based on Command Response

·DAT_BUS_WIDTH

Indicate the currently defined data bus width that was defined by SET_BUS_WIDTH command.

Table14-1:DAT_BUS_WIDTH

DAT_BUS_WIDTH	Bus Width
'00'	1 bit(default)
'01'	Reserved
'10'	4 bit width
'11'	Reserved

·SECURED_MODE

Indicates whether card is in secure mode operation.

Table14-2:SECURED_MODE

SECURED_MODE	Secured Mode Status
'0'	NOT Secured Mode
'1'	Secured Mode

·SD_CARD_TYPE

SD Card type described here.(Various SD types to be defined in the future.)

Table14-3:SD_CARD_TYPE

SD_CARD_TYPE	SD Card Type
'0000'h	SD Memory Card

·SIZE_OF_PROTECTED_AREA

Show the size of protected area.

4GB: 32,768 KB

8GB: 49,152 KB

・SPEED_CLASS

This 8-bit field indicates the Speed Class.

Table14-4:SPEED_CLASS

SPEED_CLASS	Speed Class
00h	Class 0
01h	Class 2
02h	Class 4
03h	Class 6
04h – FFh	Reserved

4GB/8GB: Class 4

・PERFORMANCE_MOVE

This 8-bit field indicates Performance of move and the value can be set by 1 [MB/sec] step.

Table14-5:PERFORMANCE_MOVE

PERFORMANCE_MOVE	Performance of Move
00h	Not Defined
01h	1 [MB/sec]
02h	2 [MB/sec]
.....	.....
FEh	254 [MB/sec]
FFh	Infinity

4GB/8GB: 2 [MB/sec]

・AU_SIZE

This 4-bit field indicates AU Size and the value can be selected in power of 2 from 16 KB.

Table14-6:AU_SIZE

AU_SIZE	Size of AU
0h	Not Defined
1h	16 KB
2h	32 KB
3h	64 KB
4h	128 KB
5h	256 KB
6h	512 KB
7h	1 MB
8h	2 MB
9h	4 MB
Ah – Fh	Reserved

4GB/8GB: 4MB

The maximum AU size, depends on the card capacity, is defined in Table 14-7.

Table14-7: Maximum AU_SIZE

Capacity	16 MB – 64 MB	128 MB-256 MB	512 MB	1 GB – 32 GB
Maximum AU Size	512 KB	1 MB	2 MB	4 MB

Application Notes:
The host should use the maximum AU Size (4 MB) to determine host buffer size.
The host can treat multiple AUs combined as one unit.

・ERASE_SIZE

This 16-bit field indicates N_{ERASE}. When N_{ERASE} numbers of AUs are erased, the timeout value is specified by ERASE_TIMEOUT. The host should determine proper number of AUs to be erased in one operation so that the host can indicate progress of erase operation.

Table14-8: ERASE_SIZE

ERASE_SIZE	Erase Size
0000h	Erase Time-out Calculation is not supported.
0001h	1 AU
0002	2 AU
0003	3 AU
.....	.....
FFFFh	65535 AU

4GB/8GB: 512AU

・ERASE_TIMEOUT

This 6-bit field indicates the T_{ERASE} and the value indicates erase timeout from offset when multiple AUs are erased as specified by ERASE_SIZE. The host can determine timeout for any number of AU erase by the Equation below.

Erase Time-out of X AU $= T_{ERASE}/N_{ERASE} \times X + T_{OFFSET}$

Table14-9: ERASE_TIMEOUT

ERASE_TIMEOUT	Erase timeout
00	Erase Time-out Calculation is not supported.
01	1 [sec]
02	2 [sec]
03	3 [sec]
…....	…....
63	63 [sec]

4GB/8GB: 42 [sec]

・ERASE_OFFSET

This 2-bit field indicates the T_{OFFSET} and one of four values can be selected. The erase offset adjusts the line by moving in parallel on the upper side. This field is meaningless if ERASE_SIZE and ERASE_TIMEOUT are set to 0.

Table14-9: ERASE_OFFSET

ERASE_OFFSET	Erase offset
0h	0 [sec]
1h	1 [sec]
2h	2 [sec]
3h	3 [sec]

4GB/8GB: 2 [sec]

7.3. Logical Format

Toshiba SD card is formatted before shipping compliant to the SD Card FILE SYSTEM SPECIFICATION.
Following parameters may be changed if the host system is not compliant with the SD Card Format Specification.
The logical format parameters are described in the Table 15, 16, 17, 18.
The data of the logical format is described in Appendix 3-1, 3-2, 3-3, 3-5.

7.3.1. SD card Capacities

Table 15: SD Card capacities

Item	Card Capacities					
	4GB		8GB			
	Sector	KB	Sector	KB	Sector	KB
Whole Capacity	7,929,856	3,964,928	15,826,944	7,913,472		
User Data Area Size	7,864,320	3,932,160	**15,728,640**	**7,864,320**		
Protected Area Size	65,536	32,768	**98,304**	**49,152**		

7.3.2. SD card System information

Table.16: SD card System information

Item		Card Capacities		
		4GB	8GB	
User Data Area	Data Boundary unit size (KB)	4,096		
	Cluster Size(KB)	32		
Protected Area	Data Boundary unit size (KB)	16		
	Cluster Size(KB)	16		

7.3.3. MBR, Boot Sector parameters

Table. 17: Master Boot Record a Partition Table

BP	Data Length	Field Name	Contents		
			4GB	8GB	
0	446	Master Boot Record	All 0x00		
446	16	Partition Table(partition1)	Refer Table 18		
462	16	Partition Table(partition2)	All 0x00		
478	16	Partition Table(partition3)	All 0x00		
494	16	Partition Table(partition4)	All 0x00		
510	2	Signature Word	0x55(BP510),0xAA(BP511)		

Table 18: Partition Table

BP	Data Length	Field Name	Contents		
			4GB	8GB	
0	1	B00t indicator	0x00		
1	1	Starting Head	2	0x82	
2	2	Starting Sector/Starting Cylinder	3/1	3/0	
4	1	System ID	0x0B		
5	1	Ending Head	30	15	
6	2	Ending Sector/Ending Cylinder	30/975	60/979	
8	4	Relative Sector	8,192	8192	
12	4	Total Sector	7,856,128	**15,720,448**	

Table.19: Extended FDC Descriptor

BP	Data Length	Field Name	Contents		
			4GB	8GB	
0	3	Jump Command	0xEB(BP0),0x00(BP1),0x90(BP2)		
3	8	Creating System Identifier	(Card Specific 8Byte-Data)		
11	2	Sector Size	512		
13	1	Sectors per Cluster	64	64	
14	2	Reserved Sector Count	6,274	4,354	
16	1	Number of FATs	2		
17	2	Number of Root-directory Entries	0		
19	2	Total Sectors	0		
21	1	Medium Identifier	0xF8		
22	2	Sectors per FAT	0	0	
24	2	Sectors per Track	63		
26	2	Number of Sides	128	255	
28	4	Number of Hidden Sectors	8,192	8,192	
32	4	Total Sectors	7,856,128	**15,720,448**	
36	4	Sectors per FAT for FAT32	959	**1,919**	
40	2	Extension Flag	0		
42	2	FS Version	0		
44	4	Root Cluster	2		
48	2	FS Info	1		
50	2	Backup Boot Sector	6		
52	12	Reserved	All 0x0		
64	1	Physical Disk Number	0x80		
65	1	Reserved	0x00		
66	1	Extended Boot Record Signature	0x29		
67	4	Volume ID Number	(Card Specific 4Byte Data)		
71	11	Volume Label	“NO NAME “		
82	8	File System Type	“FAT32“		
90	420	(Reserved for system use)	All 0x00		
510	2	Signature Word	0x55(BP510), 0xAA(BP511)		

7.3.4 FAT

FAT1 and FAT2 are consisted with the same data.

1GB / 2GB: FAT16 .

Table.20: FAT

BP	4GB	8GB	
	FAT32		
0	0xF8		
1	0xFF		
2	0xFF		
3	0xFF		
4	0xFF		
5	0xFF		
6	0xFF		
7	0x0F		
8	0xFF		
9	0xFF		
10	0xFF		
11	0x0F		
12	0x00		
….	0x00		
End	0x00		

7.3.5. Root Directory Entries

Initial values are All “0x00”.

7.3.6. User Data Area

Initial values are All “0xFF”.

8. Others: Limited Conditions, SD Specification Compliance

1) Non Supported Registers:

DSR Register (Optional register: PHISYCAL LAYER SPECIFICATION 5.6)

2) Non Supported Functions:

Programmable Card Output Driver (Optional in PHYSICAL LAYER SPECIFICATION 6.5)
Card ‘s Internal Write Protect (Optional in PHYSICAL LAYER SPECIFICATION 4.3.5.)

3) Non Specified Command:

CMD4 SET_DSR
CMD56 GEN_CMD

9. Host System Design Guidelines

The purpose of this guideline is a reference to help the design of the SD Memory Card interface of the Host system.

The description here does not make any warranty fitness for particular host.
The implementations of the host systems are different in each system.
Please design the SD Memory Card Host systems considering the each condition.

Mandate: Mandate requirement to the Host implementation
Recommendation: Recommended Implementation, Just General Example

9.1 Error handling (Recommendation)

This section shows a reference of host's error handling for errors generated in accessing the SD card.

9.1.1 Basic processing for error handling

9.1.1.1 Definition of error handling

(1) Retry process

Retry process refers to re-issuing a command. For example if SD card fails to receive a command due to noise, the command is issued again.

(2) Recovery process

Recovery process refers to the process taken by the host when SD card normally receives a command and, during the processing the command, it detects a General Error.

(3) Host's exception handling

The exception handling refers to the process taken by the host when the SD memory card normally receives a command, and during the command processing, it detects an error other than ERROR. This problem can be resolved by neither retry process nor recovery process.

9.1.1.2 Common error handling

9.1.1.2.1 Error against command response

(1) Time-out

Run the retry process. To avoid the infinite loop, implement a retry counter in the host so that, if the retry counter expires, the exception handling starts in the host.

(2) ERROR

Following the procedure per command, run the recovery process.

(3) Other errors

If the unit and size of address fail to conform to the SD memory card specification, no such errors can be resolved with command retry, requiring the exception handling by the host.

9.1.1.2.2 Process by data response

(1) Time-out

For the multiple command, send a CMD12. Response to CMD12 shall follow the procedures defined in 9.1.1.2.1.

(2) Error detection

Follow the same procedure as in (1) Time-out.

9.1.1.2.3 Clearing the error bit due to CMD13

Error handling shall be completed with checking SD_STATUS of CMD13 and read clear. Procedure from error detection to CMD13 shall be closed within one error handling so that no errors remain in a response to the next command. For issues to be noted after the time-out processing, refer to 9.2.

9.1.1.3 Error handling in SD mode

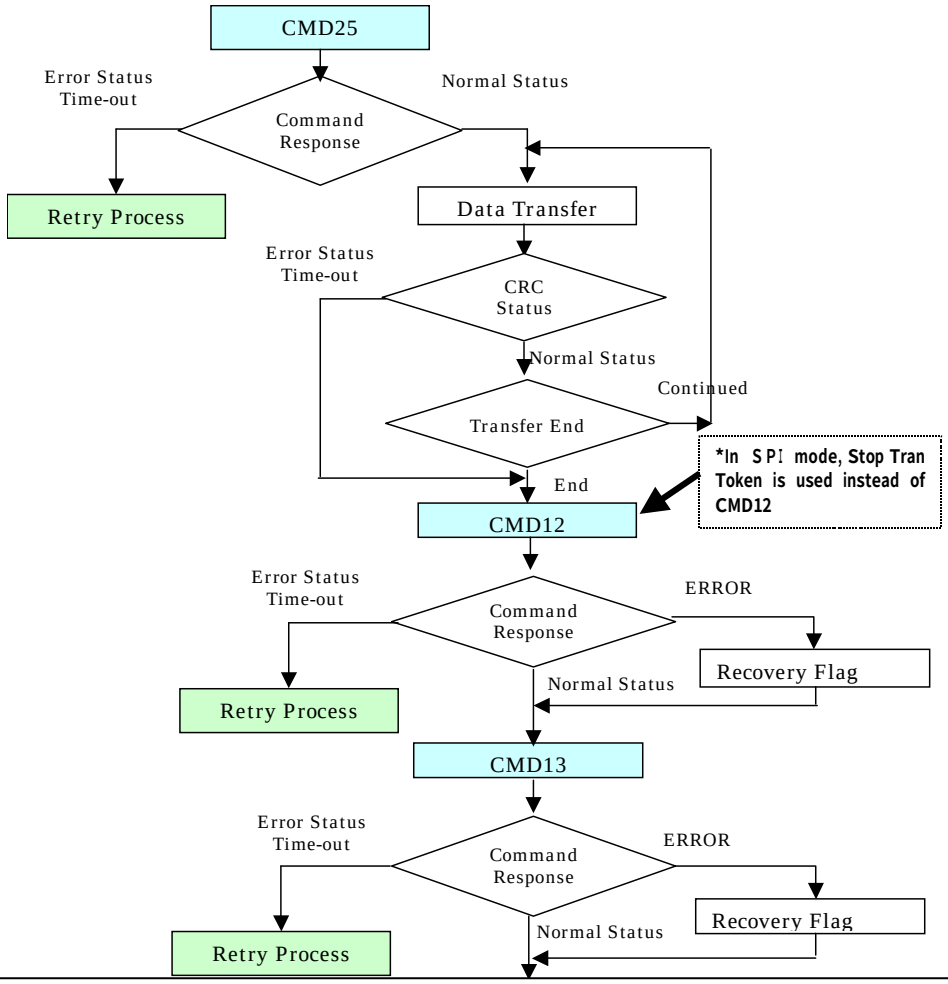
9.1.1.3.1 Error handling for WRITE_MULTIPLE_BLOCK (CMD25)

This product uses the NAND type flash memory. If the NAND type memory fails to write on a page, due to the configuration scheme, such failure may affect the data in other pages within the same delete block.

(Delete block refers to the minimum unit allowed to be deleted. It consists of multiple pages)

Thus, if CMD25 (WRITE_MULTIPLE_BLOCK) causes an error in writing multiple blocks, check the number of blocks successfully written by issuing ACMD22.

If the number of blocks successfully written differs from the expected value, some blocks may contain data not normally written. Thus, write it again. Standard flow (Figure 9), retry process flow (Figure 10), recovery process flow (Figure 11), and host's exception handling flow (Figure 12) including the error recovery for CMD25 are shown below.



(1) Writing data across the OUT_OF_RANGE boundary may expire the data CRC response timer.
(2) For an error taking place in writing, judge the condition if the recovery operation is required or not.
(3) Take the recovery action after using ACMD22 to count the blocks that was written.
(4) To the repetition process of retry and recovery operations, insert a condition for breaking the infinite loop.

Figure 9 Standard flow including the CMD25 error recovery process

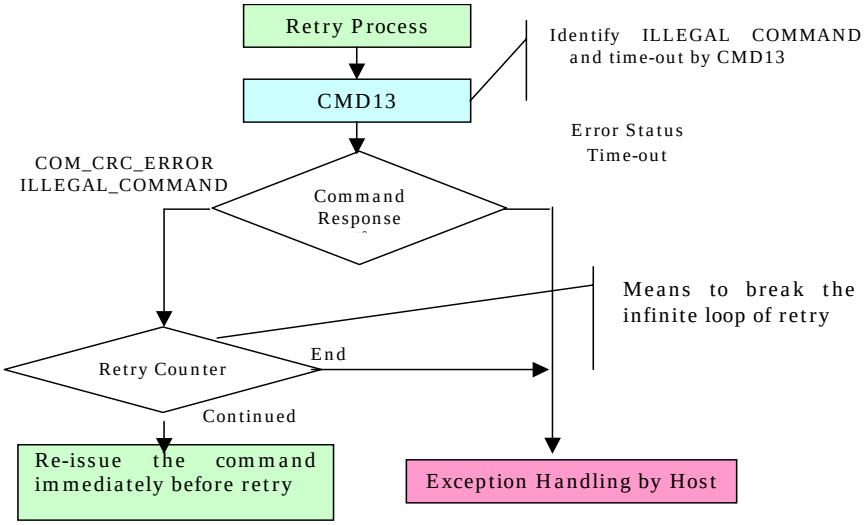


Figure 10 Retry process flow

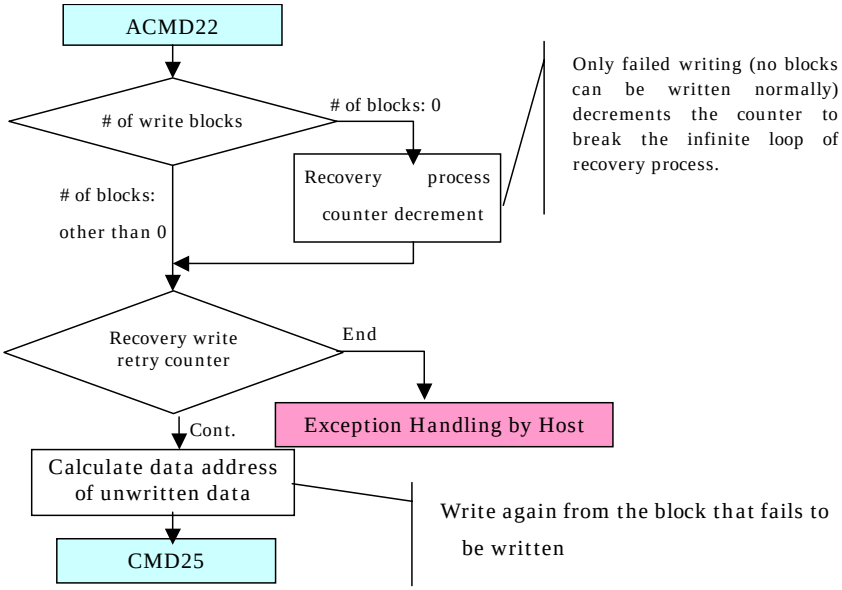


Figure 11 Recovery write flow

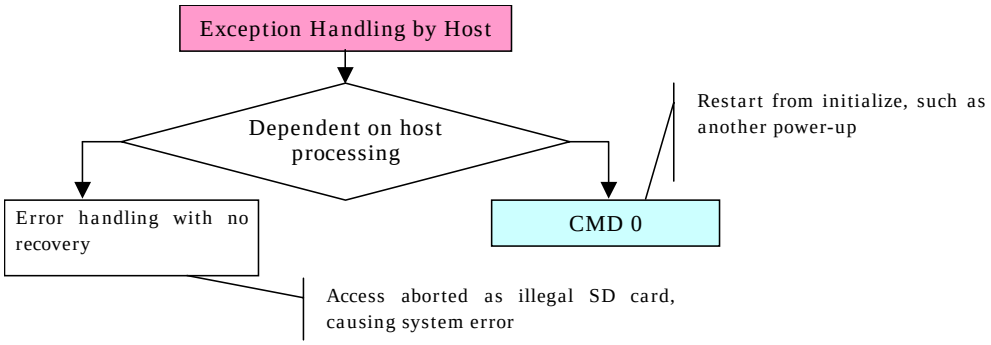


Figure 12 Flow of exception handling by host

9.1.1.3.2 Error handling for READ _MULTIPLE_BLOCK CMD18

Notes on CMD18 operations are listed below.

(1) Attempting to read the final block may cause OUT_OF_RANGE. In such case, ignore the OUT_OF_RANGE.
(2) If CARD_ECC_FAILED occurs, retry reading.
(3) Retry process shall follow Figure 13.
(4) Read recovery process shall follow Figure 14.

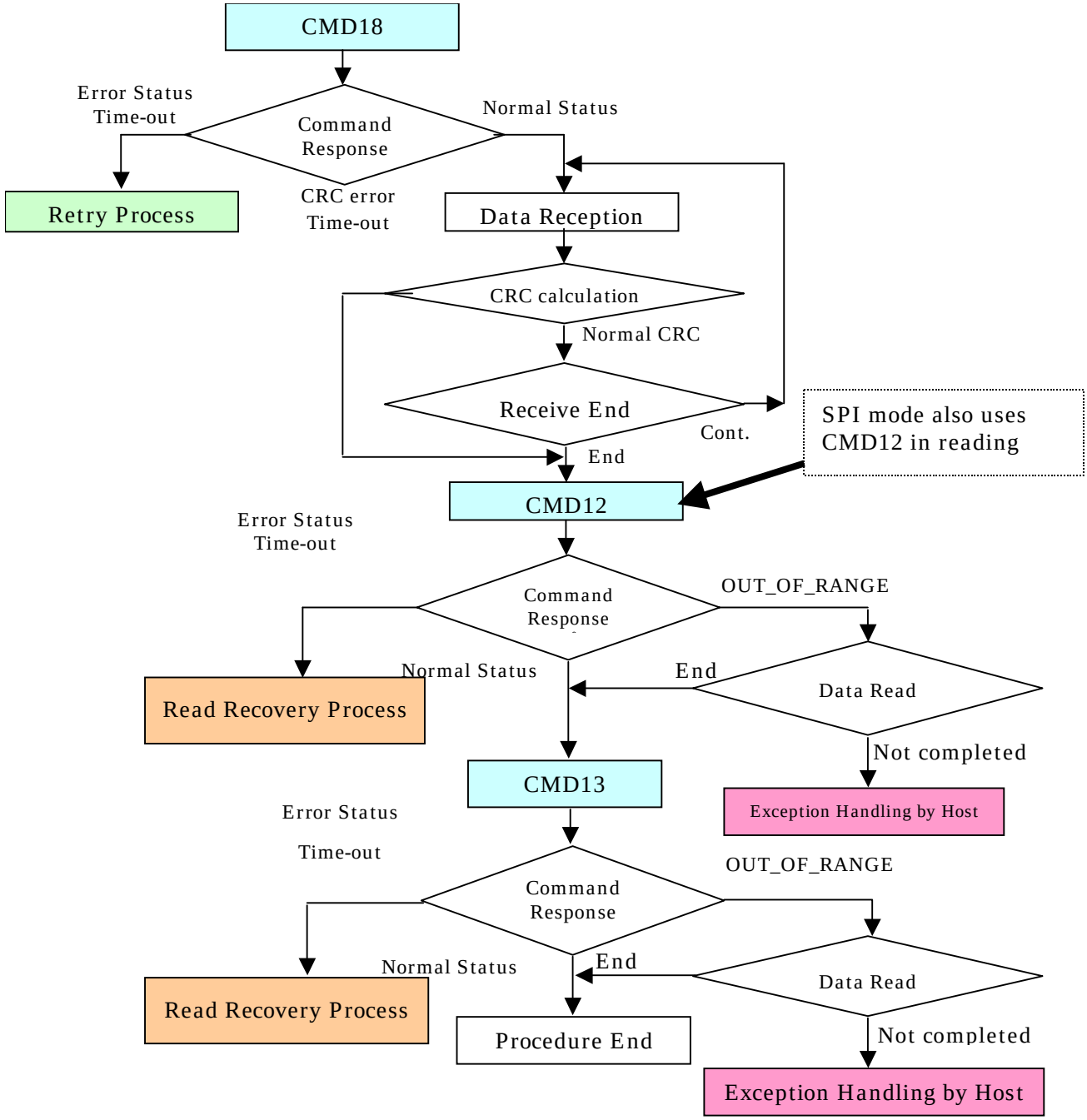


Figure 13 Standard flow including CMD18 error recovery process

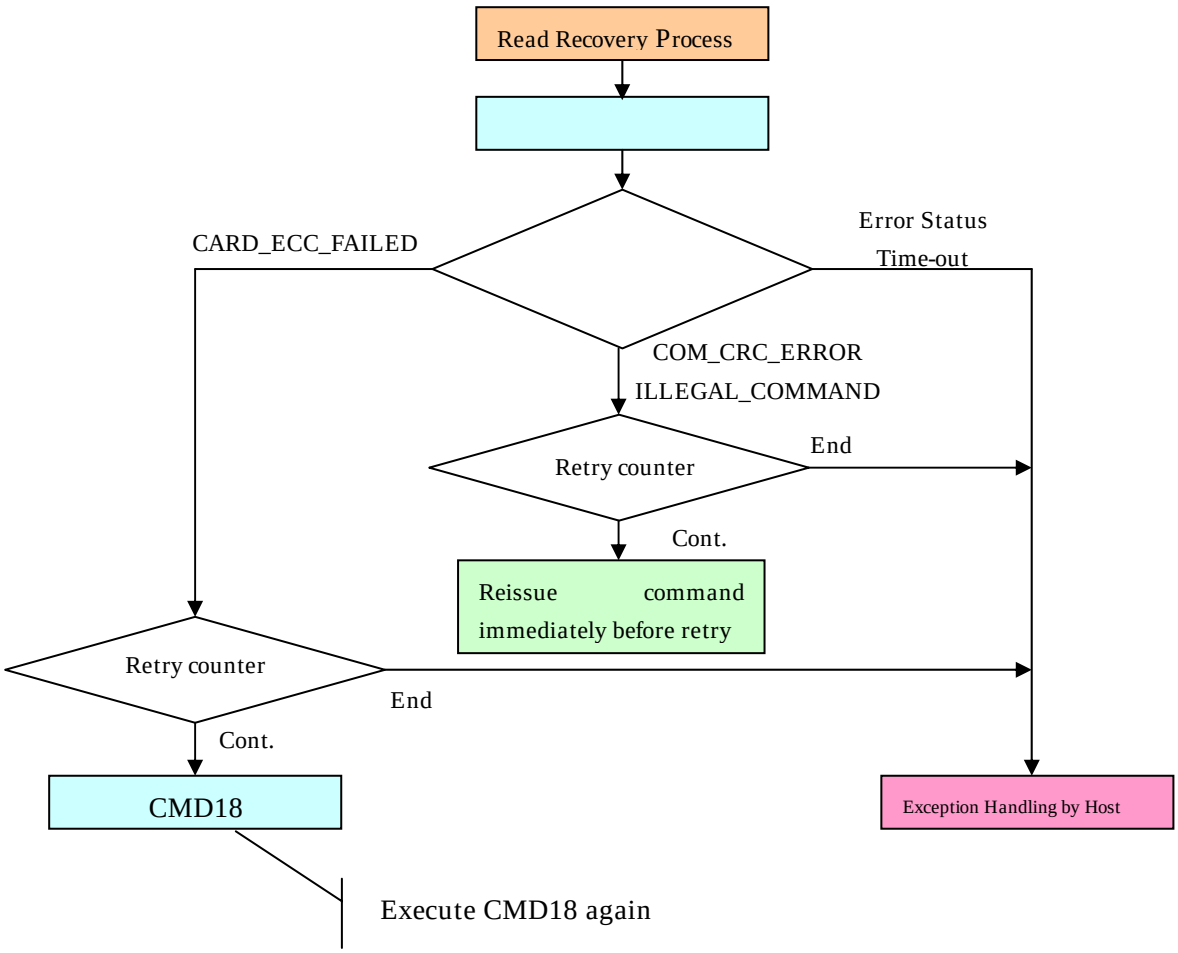


Figure 14 Read retry process flow of CMD18

9.2 Efficient Data Writing to SD Memory Card (Recommendation)

To control the SD memory card with a higher speed and lower power consumption, it is recommended that Multiple_Block_Write should be used as a command for writing data and the size of data written by each command should be the FAT cluster size×n (n: integer).

9.2.1. WRITE_SINGLE_BLOCK and WRITE_MULTIPLE_BLOCK

WRITE_SINGLE_BLOCK (CMD24) is a command used to write data of 512Bytes, which is suitable for writing comparatively small capacity of data (512byte:SingleBlock) such as updating mainly a part of File System (e.g. FAT). *1

On the other hand, WRITE_MULTIPLE_BLOCK (CMD25) is a command for writing data to blocks that have consecutive addresses per command, which is suitable to write a large capacity of data (e.g. data section in a file). Using WRITE_MULTIPLE_BLOCK to write data with a cluster unit (512Byte×128Block=64KByte) in the file system (Figure 15) is an efficient access to the flash memory, providing a higher-speed writing compared to writing the same capacity of data with Single_Block_Write (*2). In addition, this command decreases internal processes in the SD memory card, reducing the power consumption for writing a block. By avoiding the issuing command per 512 bytes as in WRITE_SINGLE_BLOCK, software processes in the host device become faster. For this operation, check that the sectors in the SD memory card and file system have compatibility as described in Figure 16.

For writing the File System (e.g. FAT Table), it is recommended to update data of minimum amount with collective units. Updating every time when the cluster chain changes frequently causes writings of small amount of data, degrading the write performance.

*1: Writing a large amount of data per block with WRITE_SINGLE_BLOCK causes updating the card system so to reliably store the 512Byte data in the flash memory, as a result, lowering the write performance and increasing the power consumption.
*2: If consecutive multiple clusters are available, efficient writing is obtained by writing 32Block (16kB)×n (n = integer).

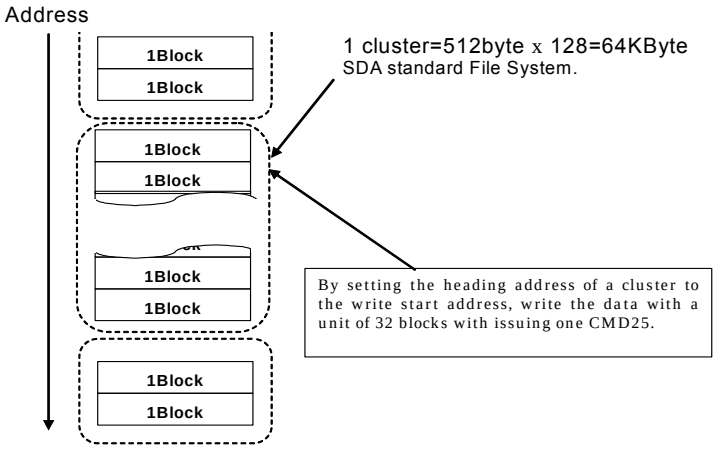


Figure 15 Writing multiple blocks with Multiple_Block_Write

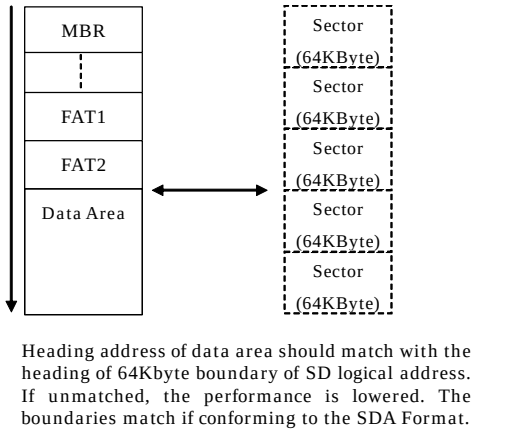


Figure 16 Matching between logical address and file system

9.2.2 Processing flow of WRITE_MULTIPLE_BLOCK

Figure 17 shows a flow chart of writing using WRITE_MULTIPLE_BLOCK command.

After issuing CMD25 and analyzing the response, write data of 512Bytes is output. Thereafter, while checking that CRC status sent from a card is normal, send the subsequent block. If the final block is sent, send Stop_Tran command (CMD12) to close the process.

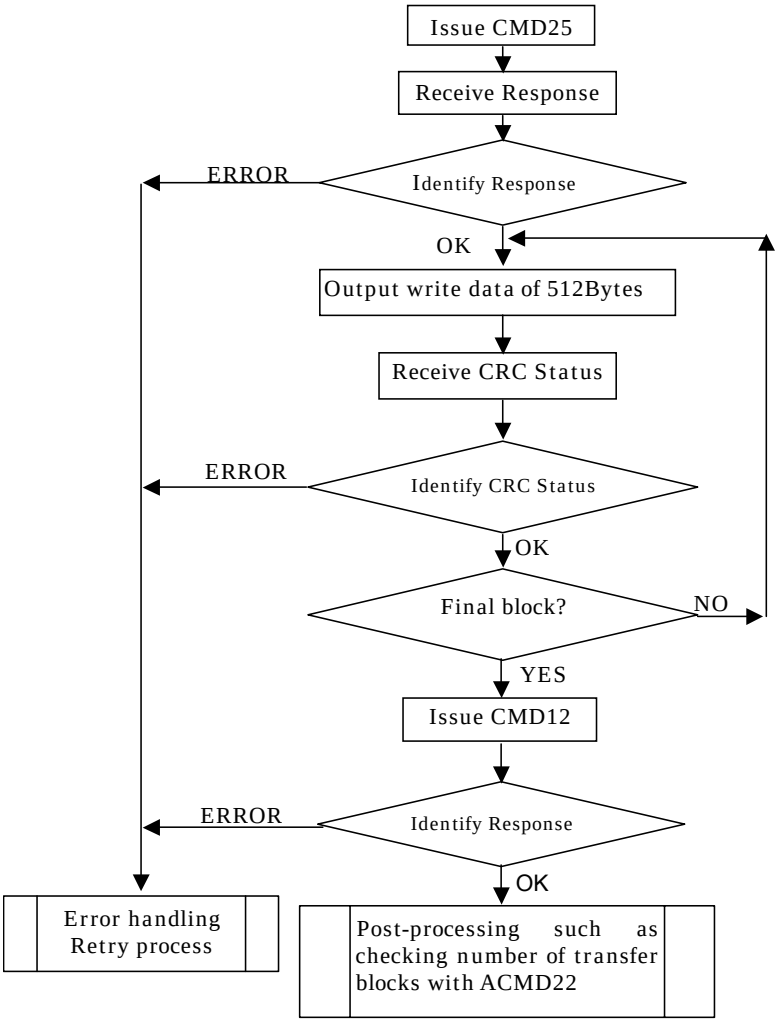


Figure 17 Write flow of WRITE_MULTIPLE_BLOCK processing

9.2.3 Power control of SD memory card (Recommended)

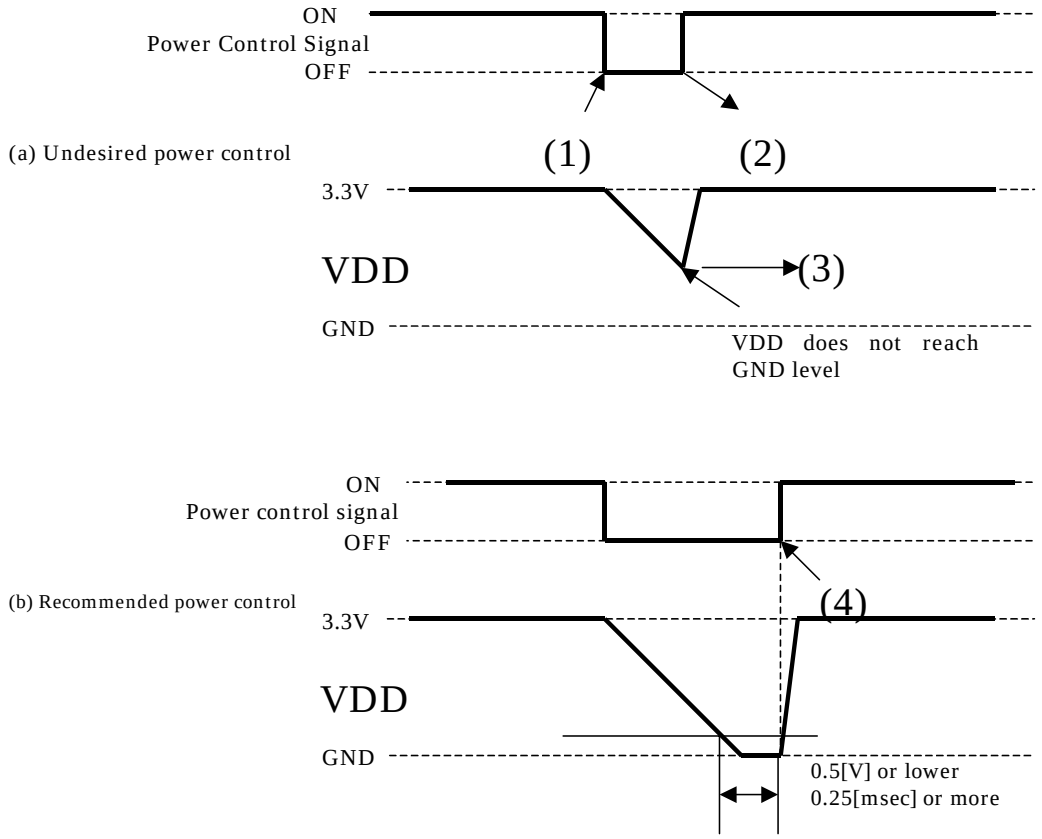
SD memory card needs the initialization time of up to 1 second *4 for power –up. In other words, once the power is turned off, the initialization time is consumed before the next read/write processes, lowering the performance. Thus, it is recommended that normally, SD slot is being turned on and the power is turned off after SD memory card has no accesses for certain duration. If SD card has no accesses, it enters the stand-by mode for saving the power consumption.

* 4: Specified in the SD Physical Specification.

Reactivate the SD memory card

In reactivating the SD memory card (turn off and on mainly for reducing the power consumption) from the host device, check in advance that the power line reaches the GND level then turn it on. If the time from power-off to power-on is too short, resetting the card may not occur normally. On the specification, power off must keep the voltage of 0.5[V] or lower for 0.25[msec] at least.

The figure below illustrates undesired and recommended cases of power control. In developing the host devices, check the power control to prevent the undesired case.



Turn off at (1) in Undesired Case in Figure (a) and restart (turn on) when VDD does not reach GND level as shown in (2), and you may fail to reset normally.
Figure (b) shows the recommended power control. Turn on at the time of (4) when VDD reaches the GND level, and you can reset the SD memory card surely with a higher reliability.

Figure 18 Power control

9.3. Retry after Memory write (Mandate)

Please issue the ACMD22 and check written blocks if it occurs error by checking the written blocks after Memory write. (CMD25: WRITE_MULTIPLE_BLOCK)
Please retry CMD25 blocks if written blocks is different from your expectation.

Background

The Flash Memory used in this card has possibility of Memory Write (Program) Error.
If the Memory Write Error occurs in some memory page, the Write error may impacts other pages in the same block.

9.4. SPI-Mode initialization (Mandate)

SD Card shall be initialized by ACMD41. Do NOT use CMD1 for SPI-Mode initialization.

9.5.SPI-Mode RSV pin Pull up(Mandate)

RSV(#8,#9 in SPI Mode) shall be pulled up by 10-100k-ohm resistors.
(See **6.1. SD Card Pins**)

9.6.Prohibition during Write (Mandate)

Do not turn off the power or remove the SD Memory Card from the slot before read/write/ mutual authentication operation is complete. Avoid using the SD Memory Card when the battery is low. Power shortage, power failure and/or removal of the SD Memory Card from the slot before read/write/mutual authentication operation is complete will cause malfunction of the SD Memory Card, loss of data and/or damage to data.

Please comment and inform this prohibition to the end users in proper way. (Manual or Instructions)

9.7.Process after Timeout in case of Read or Write (Recommendation)

If there are no-response after the timeout passed in case of read or write (Recommendation), please issue the CMD12(Stop Transmission) and stop the data transfer to prevent the host stuck on waiting for the response.

(Reference :7.3.3. Data Token, 7.3.4.Data Error Token of SD PHYSICAL LAYER SPECIFICATION.)

In case of SPI mode, there are some restrictions regarding to access the out of range boundary.

1) Response error (*1) will be occurred when host issue CMD12 over the out of range boundary under WRITE_MULTIPLE (CMD25, ACMD25) action.
   Host should neglect CMD12 error status.

2) This maybe occurred when SD CLK is low frequency.

In case of out of range token maybe duplicated, please check case (a) and case (b) when issue CMD12 after reading before the boundary using READ_MULTIPLE (CMD18, ACMD18).

(a) Response error maybe occurred (*1)
(b) Response of CMD12 maybe not issued.

- Re-issue CMD12, then next command can be received
- Neglect the response of re-issue CMD12

*1: Response Error Descriptions

- If CRC Check is On.

  Com CRC Error is responded.

- If CRC Check is Off.

  In case of 1) above, R1=0x44(Parameter Error & Illegal Command) .
  In case of 2) above, R1=0x44(Illegal Command) .

9.8. Host Timeout Setup (Recommendation)

The timeout value is recommended as below. (Table. 15.)
The memory Erase function requires the longest time before the Card Response.
The erase time for Memory Block is also included for the Timeout value in the Data erase operation in the SD Memory Card. (Table. 16)
The Host system should chose the appropriate block size considering the erase time.

Table15:Recommended Time out value

Condition	Recommended Value (Max.)
Waiting for the CMD Response	64cycles
Read Data output after issue the Commands	100ms
Busy Status Change	1s

Table16:Erase time reference value

4GB 8GB	The Host system should chose the appropriate block size considering the erase time.

NOTE: The Value in this table is Reference for setting the timeout value.

9.9. SD Command (Mandate)

1) CMD0 continuously issue

Do NOT continue the CMD0 with 1Pin(CD/DAT3)='Low' just after CMD0
or the SD Card initialized in SPI mode.
In case of 1 pin (CD/DAT3)="Low", it means SPI mode so be careful to the duration of CMD0 issue.
Please choose the appropriate timing interval for CMD0 to prevent this problem.
The interval is related with the pull up Resister value. of the host side.

2) After the Security Read Command

Please issue the CMD13 to ensure the status change to the transmission state
or wait more than 100 us, after issue the ACMD18 or ACMD43.

3) CMD12(SD mode) or 'Stop Tran Token'(SPI mode) after Multiple Block Write Command

When the CMD12(STOP_TRANSMISSION, SD mode) or 'Stop Tran Token' (SPI mode) is issued after Multiple Block Write Command (CMD25, ACMD25), please issue the CMD12 or 'Stop Tran Token' immediately(*) after the last data block, to complete the data write transaction soon.
(*)It should be within 400usec after the end of BUSY status for the last data block.

4) Time Interval between successive SD commands

Time interval between the BUSY end of the SD command and the start bit of the next SD command should be more than 15usec.
If the time interval is less than 15usec, SD bus error or device operation error may occur occasionally.

9.10. Pull Up resistors (Recommendation)

CMD and DAT [3:0] can pull up with 10-100k ohm resistors by the host side.
Pleased disable the Card-Internal pull up on CD by ACMD42 before access. (Refer Fig. 7)

9.11. Write/ Erase Size management: (Recommendation)

1) Erase Unit

The erase size is recommended to using Boundary unit indicated by Erase Sector size below.

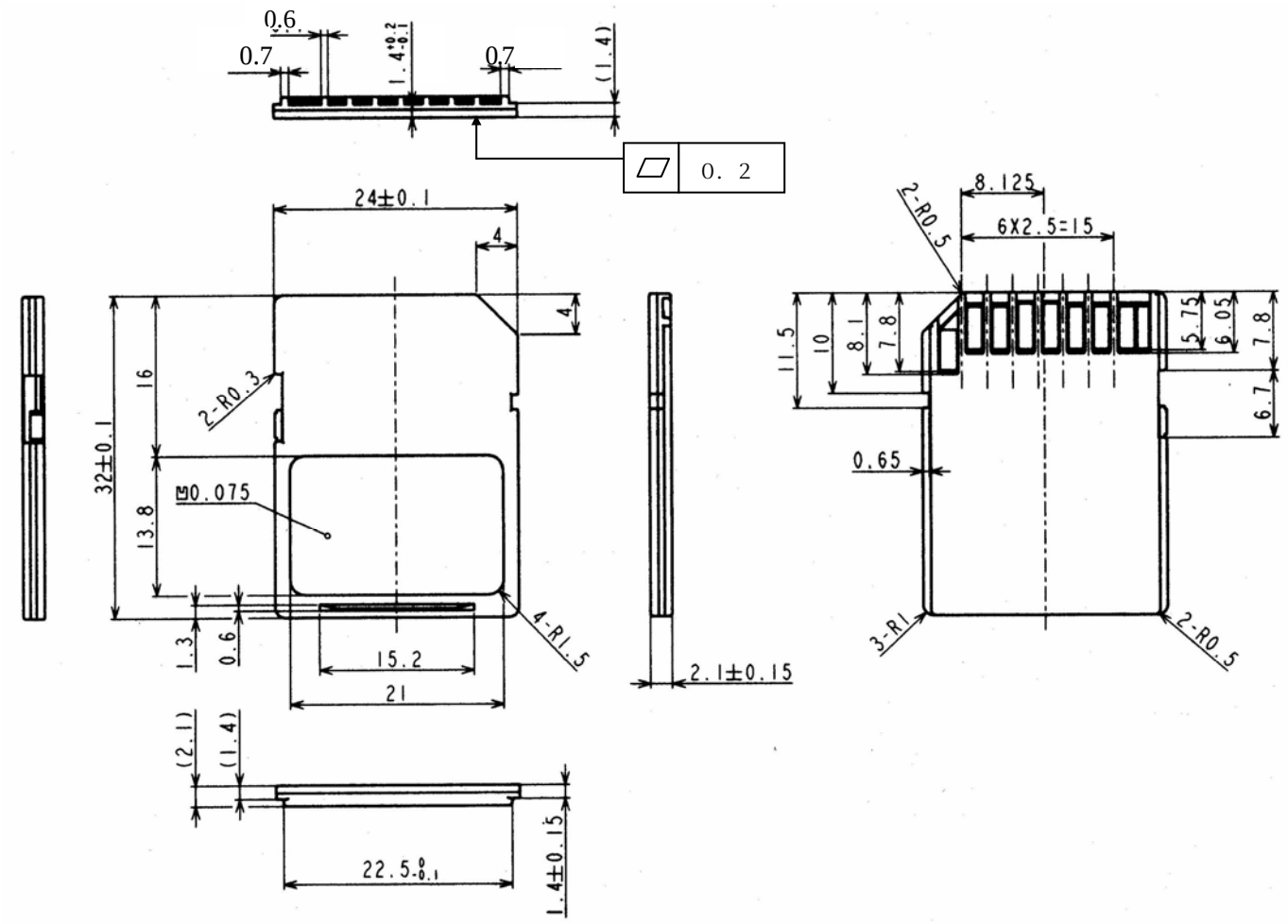
The erase unit size is given as below.

Erase Sector Size = Block_length x (SECTOR_SIZE) = 512 Byte x 128 -block= 64 K Byte
(Block_length can calculate from WRITE_BL_LEN)

2) Faster Write

Multiple block write by command :WRITE_MULTIPLE(CMD25,ACMD25) allows faster data write.

Appendix 1. SD Card Mechanical Dimensions (Unit: mm)



Tolerance±0.15

Appendix 2-1: initial value of OCR Register

4GB

Field	C	C	RSV			3.6 - 1.6									RSV	
Bit Position	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Binary	*	1	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Hexadecimal	*		0		F		F		8		0		0		0																	

2.7V - 3.6V operation

8GB

Field	C	RSV				3.6 - 1.6									RSV	
Bit Position	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Binary	*	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Hexadecimal	*		0		F		F		8		0		0		0																	

2.7V - 3.6V operation

Appendix 2-2 : initial value of CID Register

4GB

Field	MID		OID				PNM										PRV		PSN								RSV	MDT			CRC7	1
Bit Position	127	126	125	124	123	122	121	120	119	118	117	116	115	114	113	112	111	110	109	108	107	106	105	104	103	102	101	100	99	98	97	96
	95	94	93	92	91	90	89	88	87	86	85	84	83	82	81	80	79	78	77	76	75	74	73	72	71	70	69	68	67	66	65	64
	63	62	61	60	59	58	57	56	55	54	53	52	51	50	49	48	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32
	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Binary	0000	0010	0101	0100	0100	1101	0101	0011	0100	0100	0011	0000	0011	0100	0100	0111	****	****	****	****	****	****	****	****	****	****	0000	****	****	****	#######	1
Hexadecimal	0	2	5	4	4	D	5	3	4	4	3	0	3	4	4	7	*	*	*	*	*	*	*	*	*	*	0	*	*	*	#	#

8GB

Field	MID		OID				PNM										PRV		PSN								RSV	MDT			CRC7	1
Bit Position	127	126	125	124	123	122	121	120	119	118	117	116	115	114	113	112	111	110	109	108	107	106	105	104	103	102	101	100	99	98	97	96
	95	94	93	92	91	90	89	88	87	86	85	84	83	82	81	80	79	78	77	76	75	74	73	72	71	70	69	68	67	66	65	64
	63	62	61	60	59	58	57	56	55	54	53	52	51	50	49	48	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32
	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Binary	0000	0010	0101	0100	0100	1101	0101	0011	0100	0100	0011	0000	0011	1000	0100	0111	****	****	****	****	****	****	****	****	****	****	0000	****	****	****	#######	1
Hexadecimal	0	2	5	4	4	D	5	3	4	4	3	0	3	8	4	7	*	*	*	*	*	*	*	*	*	*	0	*	*	*	#	#

Appendix 2-3 : initial value of CSD Register

4GB

Field	CS	RSV	TAAC	NSAC	TRAN SPEED	CCC	READ_	R	W	R	D	RSV	C_SIZE	R	E	SECTOR_SIZ	WP_GRP_SIZ	W	RS	R2W_	WRITE_	W	RSV	F	C	P	T	FIL	RS	CRC7	1
Bit Position	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	2	2	1	1	0	9	8	7	6	5	4	3	2	1	0	9	8	7	6	5	4	3	2	1	0	9	8	7	6	5	4
	7	0	9	6	3	2	1	0	9	6	3	2	1	0	7	4	3	2	1	0	9	6	5	4	3	2	1	0	7	0	1
Binary	0100	0000	0000	1110	0000	0000	0011	0010	0101	1011	0101	1001	0000	0000	0000	0000	0001	1101	1111	1111	0111	1111	1000	0000	0000	1010	0100	0000	0000	0000	#######
Hexadecimal	4	0	0	E	0	0	3	2	5	B	5	9	0	0	0	0	1	D	F	F	7	F	8	0	0	A	4	0	0	0	##

8GB

Field	CS	RSV	TAAC	NSAC	TRAN SPEED	CCC	READ_	R	W	R	D	RSV	C_SIZE	R	E	SECTOR_SIZ	WP_GRP_SIZ	W	RS	R2W_	WRITE_	W	RSV	F	C	P	T	FIL	RS	CRC7	1
Bit Position	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	2	2	1	1	0	9	8	7	6	5	4	3	2	1	0	9	8	7	6	5	4	3	2	1	0	9	8	7	6	5	4
	7	0	9	6	3	2	1	0	9	6	3	2	1	0	7	4	3	2	1	0	9	6	5	4	3	2	1	0	7	0	1
Binary	0100	0000	0000	1110	0000	0000	0011	0010	0101	1011	0101	1001	0000	0000	0000	0000	0011	1011	1111	1111	0111	1111	1000	0000	0000	1010	0100	0000	0000	0000	#######
Hexadecimal	4	0	0	E	0	0	3	2	5	B	5	9	0	0	0	0	3	B	F	F	7	F	8	0	0	A	4	0	0	0	##

Appendix 2-4 : initial value of SCR Register

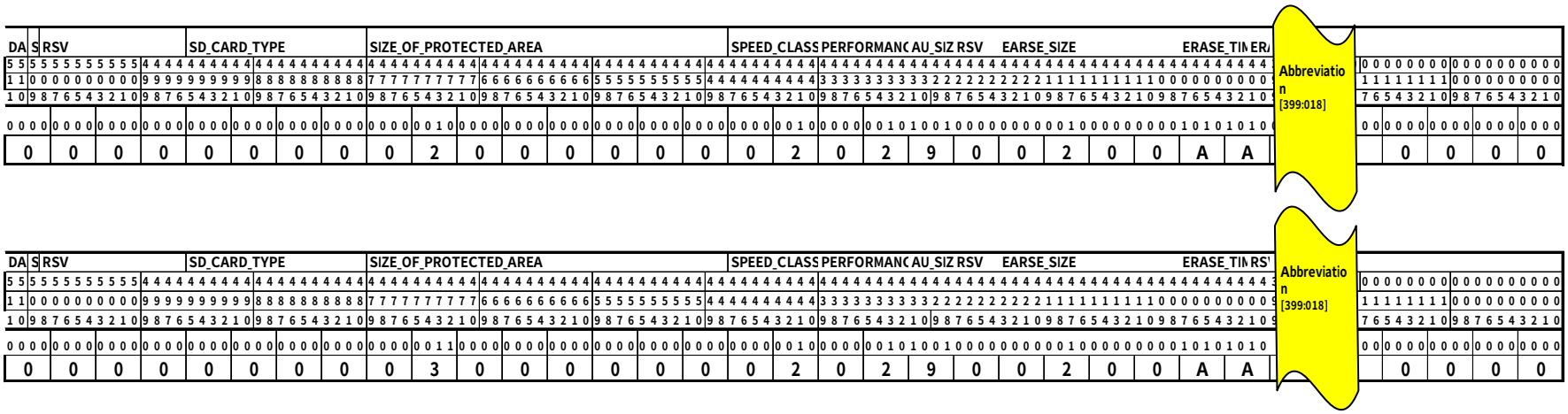
4GB

Field	SCR_S	SD_SP	D	SD_S	SD_BU	RSV				reserved for manufacturer usage							
Bit Position	63-60	59-56		55-52	51-48	47-40	39-32	31-24	23-16	15-12	11-8	7-4	3-0				
Binary	0000	0010		1011	0101	0000	0000	0000	0000	0000	0000	0000	0000	0000	0000	0000	0000
Hexadecimal	0	2		B	5	0	0	0	0	#	#	#	#	#	#	#	#

8GB

Field	SCR_S	SD_SP	D	SD_S	SD_BU	RSV				reserved for manufacturer usage							
Bit Position	63-60	59-56		55-52	51-48	47-40	39-32	31-24	23-16	15-12	11-8	7-4	3-0				
Binary	0000	0010		1011	0101	0000	0000	0000	0000	0000	0000	0000	0000	0000	0000	0000	0000
Hexadecimal	0	2		B	5	0	0	0	0	#	#	#	#	#	#	#	#

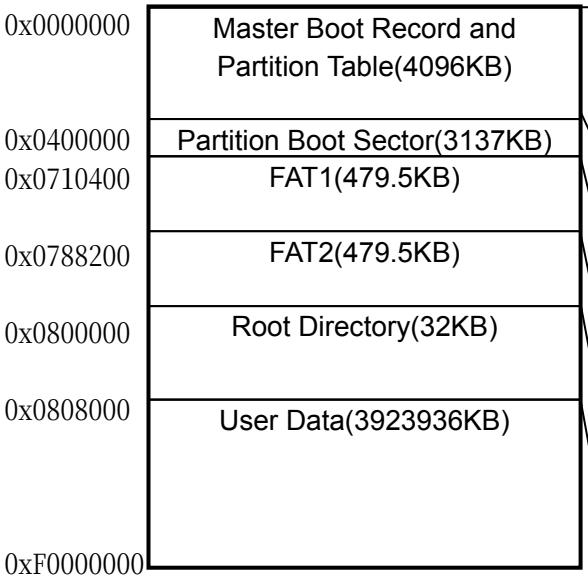
Appendix 2-5: initial value of SD Status



Appendix 3-1 : Memory Map and Dump Data of User Data Area

Last address of this memory map indicates “actual last address + 1”.

(1)4GB Card

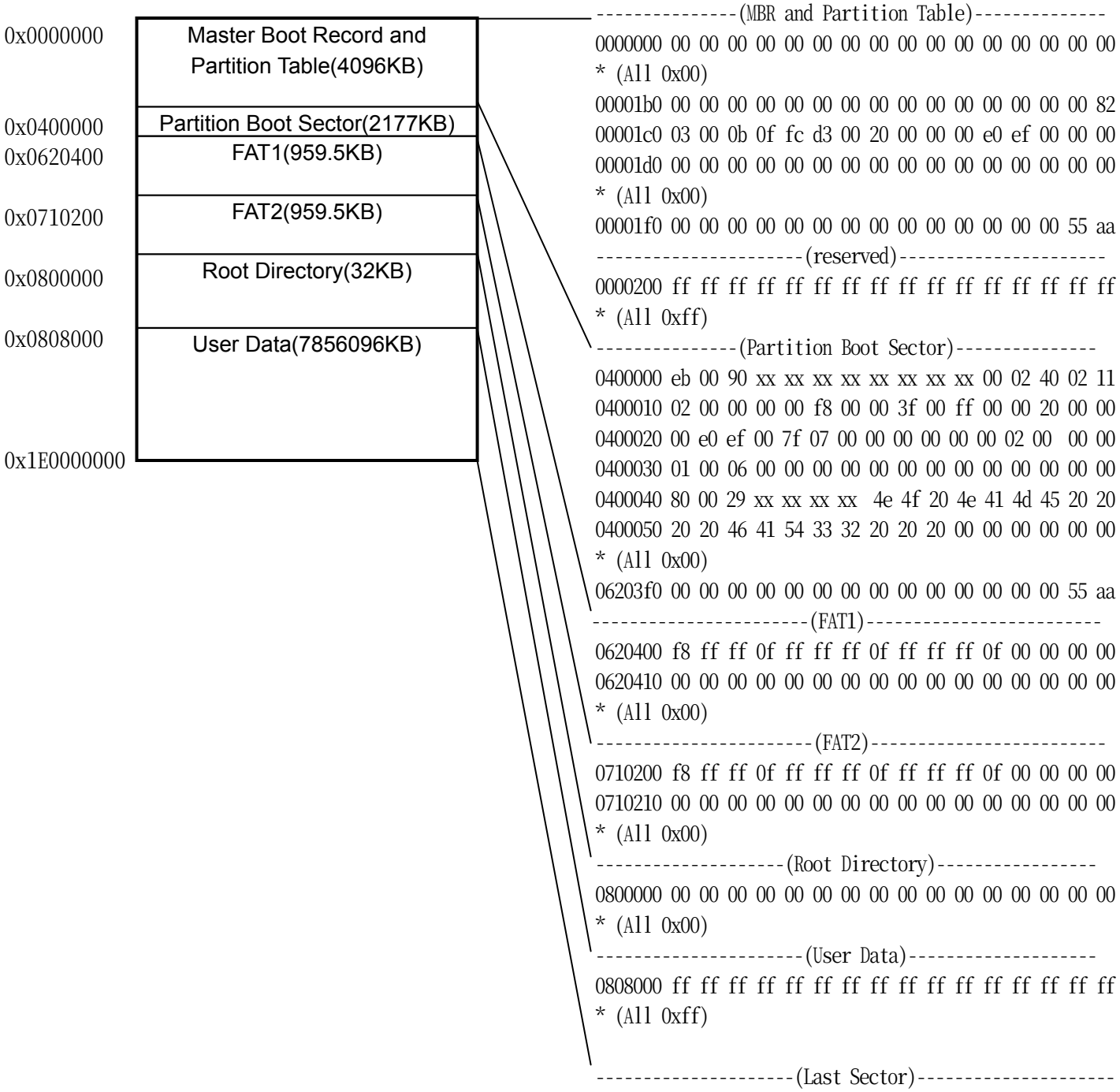



```
ADDRESS 00 01 02 03 04 05 06 07 08 09 0A 0B 0C 0D 0E 0F
---------------(MBR and Partition Table)--------------
0000000 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
* (All 0x00)
00001b0 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 02
00001c0 03 01 0b 1e de cf 00 20 00 00 00 00 77 00 00 00
00001d0 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
* (All 0x00)
00001f0 00 00 00 00 00 00 00 00 00 00 00 00 00 00 55 aa
----------------------(reserved)----------------------
0000200 ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff
* (All 0xff)
---------------(Partition Boot Sector)---------------
0400000 eb 00 90 xx xx xx xx xx xx xx xx 00 02 40 82 18
0400010 02 00 00 00 00 f8 00 00 3f 00 80 00 00 20 00 00
0400020 00 e0 77 00 bf 03 00 00 00 00 00 00 02 00 00 00
0400030 01 00 06 00 00 00 00 00 00 00 00 00 00 00 00 00
0400040 80 00 29 xx xx xx xx 4e 4f 20 4e 41 4d 45 20 20
0400050 20 20 46 41 54 33 32 20 20 20 00 00 00 00 00 00
* (All 0x00)
07103f0 00 00 00 00 00 00 00 00 00 00 00 00 00 00 55 aa
-----------------------(FAT1)-----------------------
0710400 f8 ff ff 0f ff ff ff 0f ff ff ff 0f 00 00 00 00
0710410 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
* (All 0x00)
-----------------------(FAT2)-----------------------
0788200 f8 ff ff 0f ff ff ff 0f ff ff ff 0f 00 00 00 00
0788210 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
* (All 0x00)
--------------------(Root Directory)-----------------
0800000 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
* (All 0x00)
----------------------(User Data)--------------------
0808000 ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff
* (All 0xff)

--------------------(Last Sector)---------------------
```

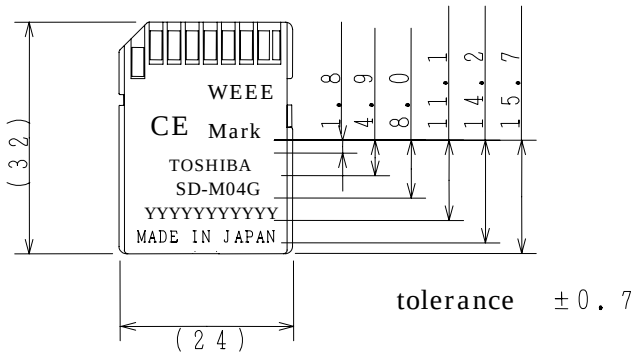
“xx” depends on SD card.

(1)8GB Card



"xx" depends on SD card.

Appendix4-1：Laser marking



CE part:

WEEE Mark:

1LINE: SPACE

2LINE: TOSHIBA

3LINE:

CAPACITY	MODEL NAME	Origin Country	LASER MARKING
4GB	SD-M04G7B7 (VDC)	JAPAN	SD-M04G
4GB	SD-M04G7B7 (VDCCN)	JAPAN	SD-M04G
4GB	SD-M04G7B7K (VDC)	TAIWAN	SD-M04G
8GB	SD-M08G7B7 (VDC)	JAPAN	SD-M08G
8GB	SD-M08G7B7 (VDCCN)	JAPAN	SD-M08G
8GB	SD-M08G7B7K (VDC)	TAIWAN	SD-M08G

4LINE: LOT NUMBER
11LETTERS
first 2letters : year
second 2letters :weekly code
others : lot number

5LINE:
MADE IN JAPAN/MADE IN TAIWAN

Appendix4-2：For Instruction Manual

Please comment and inform this prohibition to the end users in proper way. (Manual or Instructions).

Notes on usage

(1)The SD memory card includes a built-in non-volatile semiconductor memory (NAND type Flash EEP-ROM).Under normal circumstances data stored on the SD memory card cannot be corrupted or lost. If the card is used in ways other than described in these instruction manual, however, data could be corrupted or lost. Please note that **** Corporation accepts no responsibility for corruption or loss of data stored on the SD memory card, regardless of the type or cause of the problem or damage.

(2)The SD memory card is a storage medium that conforms to SDMI (Secure Digital Music Initiative) standards for protecting the rights of copyright holders. Based on SD memory card specifications, part of the memory is used as the system area, so the actually usable memory capacity is lower than the indicated capacity.

(3)The SD memory card is already formatted. If you should want to reformat it, however, do so on a device including the SD logo mark and equipped with an SD memory card formatting function. Formatting the SD memory card on other devices (computers, etc.) may result in problems, such as the inability to read or write data.

(4)Routine performance of backing-up data is strongly recommended.

Exemption Clauses

(1)**** Corporation bears no responsibility in the case of damages arising from earthquakes, fire not liable to Toshiba Corporation, operation by third parties, other accidents, or use under abnormal conditions including erroneous or improper operation and other problems.

(2)****Corporation bears no responsibility for incidental damages (lost profit, work interruption, corruption or loss of the memory contents, etc.) arising from the use of or the inability to use this unit.

(3)**** Corporation accepts no liability whatsoever for any damages arising from not having followed the descriptions in this Instruction Manual.

(4)**** Corporation accepts no liability whatsoever for any damages arising from malfunctions arising from combination with equipment or software that is not related to **** Corporation.

Cautions

(1)Keep out of reach of small children.

(2)Do not touch or have metal objects touch the terminals or connectors. Static electricity may cause malfunction, and/or loss of data.

(3)Do not bend or force the SD Card into the slot. Do not drop the SD Card onto hard surface. Doing so may cause malfunction, and/or loss of data.

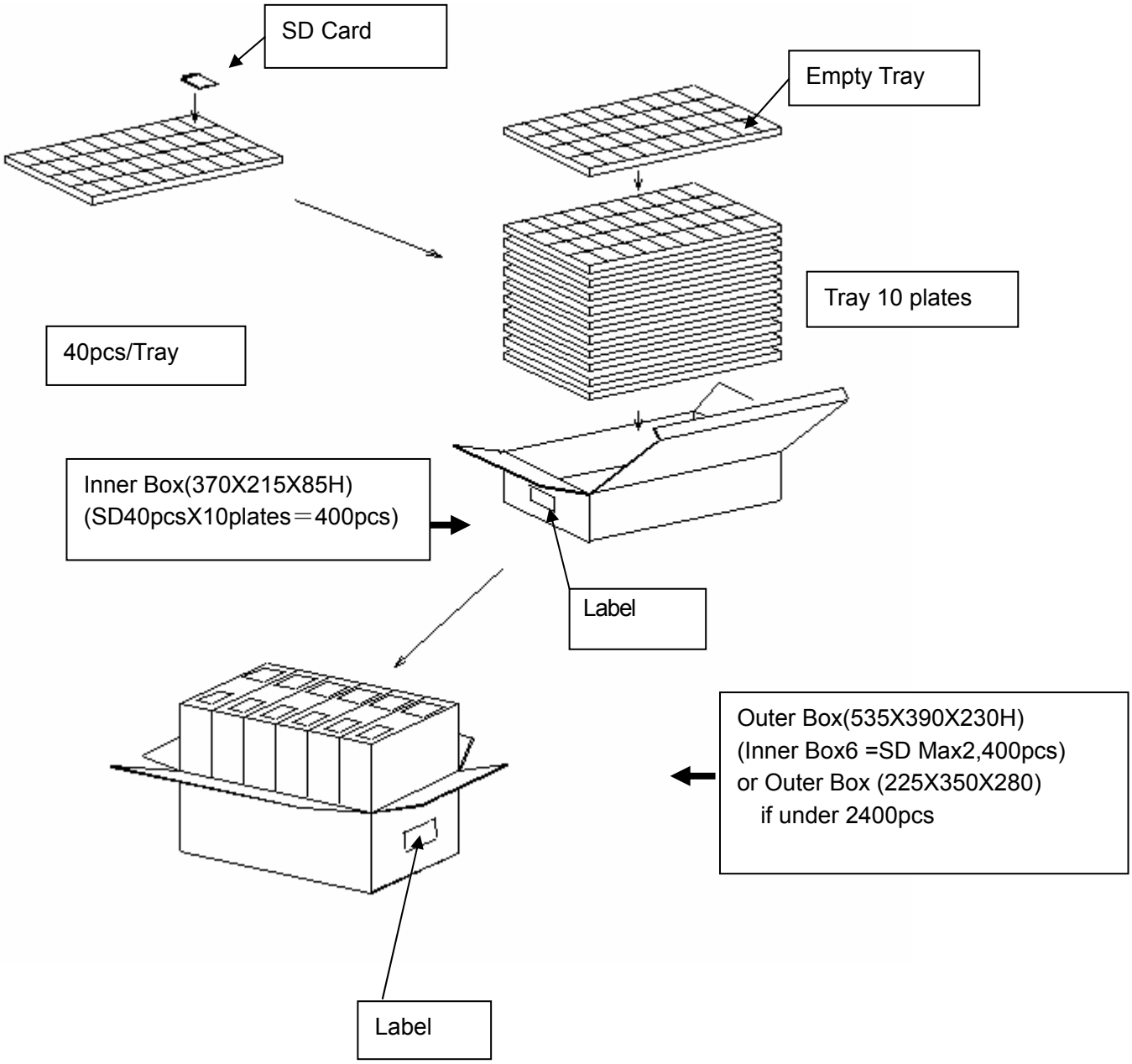
(4)Do not disassemble, transform and/or alter the SD Card.

(5)Keep away from dampness.

(6)Do not turn off the power or remove the SD Memory Card from the slot before read/write operation is complete. Avoid using the SD Memory Card when the battery is low. Power shortage, power failure and/or removal of the SD Memory Card from the slot before read/write operation is complete will cause malfunction of the SD Memory Card, loss of data and/or damage to data.

(7)The SD Memory Card is already formatted. However, if you should want to reformat it, make a back-up copy of the data stored on the SD Card prior to reformatting. WARNING: Reformatting clears all the data on the SD Card.

Appendix5-1：Package



Appendix5-2：LABEL DETAIL（400pcs BOX、2,400pcs BOX）

MODEL NAME：SD-M04G7B7 (VDCCN)　2006/30WEEK　2400pcs

TYPE	SD-M04G7B7		
ADD.C	VDCCN	Q'TY	2400PCS
NOTE　0630KVZ – 2400			
TD0001			

Y20++++++++++++++++++++++++++++++

TOSHIBA　　MADE IN JAPAN

Week CODE+3LETTERS+Q'TY

Key No

more than 3mm SPACE
at right and left

In case of SD-M04G7B7K (VDC)
and SD-M08G7B7K (VDC),
"MADE IN TAIWAN"

1）Model Name

Model Name	TYPE	ADD.C	Capacity
SD-M04G7B7 (VDC)	SD-M04G7B7	VDC	4GB
SD-M04G7B7 (VDCCN)	SD-M04G7B7	VDCCN	4GB
SD-M04G7B7K (VDC)	SD-M04G7B7K	VDC	4GB
SD-M08G7B7 (VDC)	SD-M08G7B7	VDC	8GB
SD-M08G7B7 (VDCCN)	SD-M08G7B7	VDCCN	8GB
SD-M08G7B7K (VDC)	SD-M08G7B7K	VDC	8GB

2）LOT

For the control of production or shipment
Different by production and shipment

3）Quantity

＊Inner Box
Max 400pcs
（including dummy tray according to circumstances）

＊Outer Box
Max 2,400pcs
（including empty box or buffer materials according to circumstances）

Appendix 6：FACTORY, PRODUCING COUNTRY

MODEL NAME	SD-M04G7B7 (VDC) SD-M08G7B7 (VDC)	SD-M04G7B7 (VDCCN) SD-M08G7B7 (VDCCN)	SD-M04G7B7K (VDC) SD-M08G7B7K (VDC)
ASSEMBLY,TEST	TOSHIBA MISAWA MEDIA DEVICES CO., LTD	KUNIMI MEDIA DEVICE CO.,LTD	KINGSTON TECHNOLOGY CO.,
SHIPMENT	TOSHIBA YOKKAICHI OPERATION	TOSHIBA YOKKAICHI OPERATIONS	TOSHIBA YOKKAICHI OPERATIONS
PRODUCING COUNTRY	JAPAN	JAPAN	TAIWAN

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